



Kinetis K66 Sub-Family

180 MHz ARM® Cortex®-M4F Microcontroller.

The K66 sub-family members provide greater performance, memory options up to 2 MB total flash and 256 KB of SRAM, as well as higher peripheral integration with features such as Dual USB and a 10/100 Mbit/s Ethernet MAC. These devices maintain hardware and software compatibility with the existing Kinetis family. This product also offers:

- Integration of a High Speed USB Physical Transceiver
- Greater performance flexibility with a High Speed Run mode
- Smarter peripherals with operation in Stop modes

MK66FN2M0VMD18
MK66FX1M0VMD18
MK66FN2M0VLQ18
MK66FX1M0VLQ18



144 MAPBGA (MD)
13 mm x 13 mm Pitch 1
mm

144 LQFP (LQ)
20 mm x 20 mm Pitch
0.5 mm

Performance

- Up to 180 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit

System and Clocks

- Multiple low-power modes to provide power optimization based on application requirements
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference

Security

- Hardware random-number generator
- Supports DES, AES, SHA accelerator (CAU)
- Multiple levels of embedded flash security

Timers

- Four Periodic interrupt timers
- 16-bit low-power timer
- Two 16-bit low-power timer PWM modules
- Two 8-channel motor control/general purpose/PWM timers
- Two 2-ch quad decoder/general purpose timers
- Real-time clock

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- General-purpose input/output

Memories and memory expansion

- Up to 2 MB program flash memory on non-FlexMemory devices with 256 KB RAM
- Up to 1 MB program flash memory and 256 KB of FlexNVM on FlexMemory devices
- 4 KB FlexRAM on FlexMemory devices
- FlexBus external bus interface and SDRAM controller

Analog modules

- Two 16-bit SAR ADCs and two 12-bit DAC
- Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Voltage reference 1.2V

Communication interfaces

- Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
- USB high-/full-/low-speed On-the-Go with on-chip high speed transceiver
- USB full-/low-speed OTG with on-chip transceiver
- Two CAN, three SPI and four I2C modules
- Low Power Universal Asynchronous Receiver/Transmitter 0 (LPUART0) and five standard UARTs
- Secure Digital Host Controller (SDHC)
- I2S module

Operating Characteristics

- Voltage/Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C



Ordering Information 1

Part Number	Memory		Maximum number of I/O's
	Flash	SRAM	
MK66FN2M0VMD18	2 MB	256 KB	100
MK66FX1M0VMD18	1.25 MB	256 KB	100
MK66FN2M0VLQ18	2 MB	256 KB	100
MK66FX1M0VLQ18	1.25 MB	256 KB	100

1. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K66P144M180SF5RMV2 ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_0N65N ¹
Package drawing	Package dimensions are provided in package drawings.	• MAPBGA 144-pin : 98ASA00222D¹ • LQFP 144-pin: 98ASS23177W¹

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	−55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	−2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	−500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	−100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

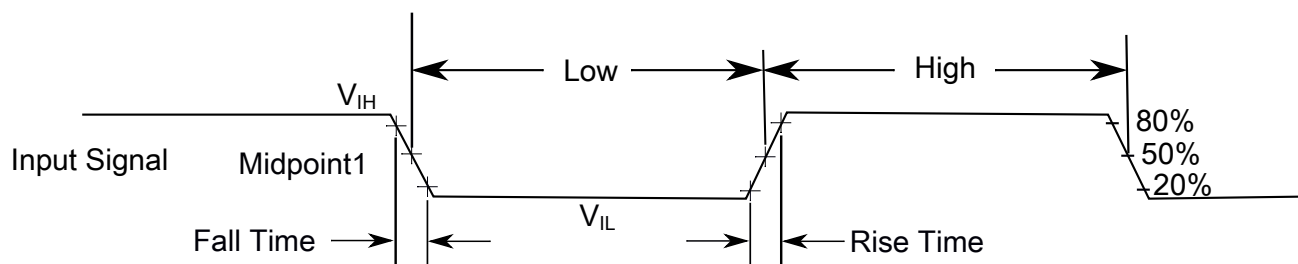
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital ¹ input voltage, including RESET_b	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹ input voltage, including EXTAL32 and XTAL32	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (digital output pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	-0.3	3.63	V
V_{USB1_VBUS}	USB1_VBUS detect voltage	-0.3	6.0	V
VREG_IN0, VREG_IN1	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Digital pins have a general purpose I/O port assigned (e.g. PTA0). Analog pins do not have an associated general purpose I/O port.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

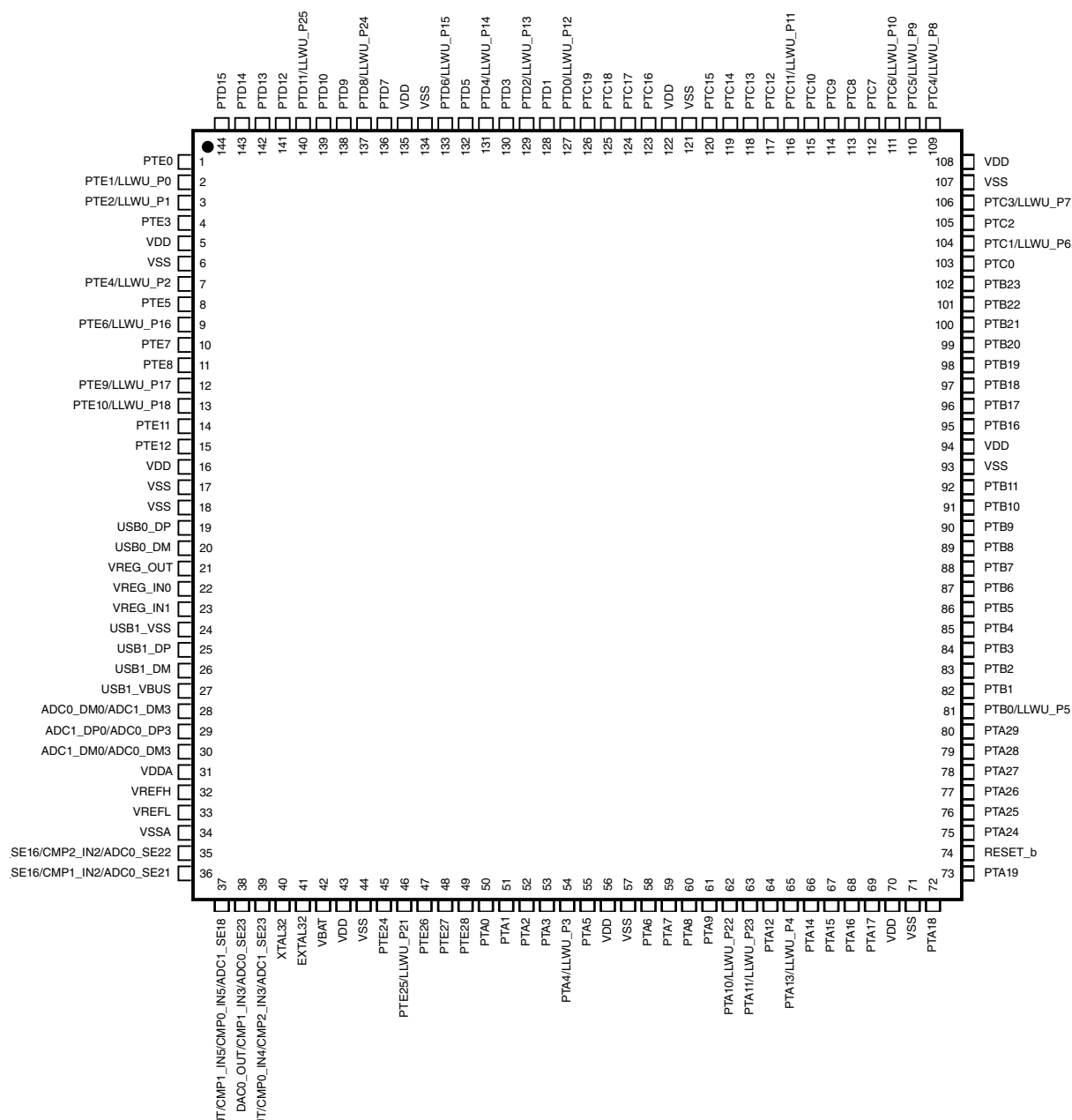


Figure 39. K66 144 LQFP Pinout Diagram