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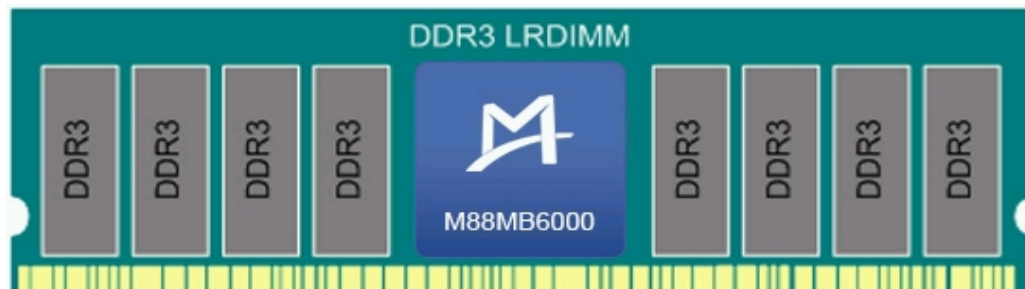
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M88MB6000 - DDR3 Memory Buffer (MB)

M88MB6000 is a Load Reduced DIMM (LRDIMM) Memory Buffer (MB) that supports DDR3 SDRAM main memory. The MB allows buffering of memory traffic to support large memory capacities. Unlike DDR3 Register Buffer (SSTE32882), which only buffers Command, Address, Control and Clock, the MB also buffers the Data (DQ) interface between the Memory Controller and the DRAM components, and has extra features such as ODT processing, rank multiplication, address mirroring, control registers accessible over SMBus, and advanced test and calibration capabilities, etc. As the data electrical load is reduced for the Memory Controller interface, the system can now support more DIMMs per channel at a faster speed and higher density. All memory control for the DRAM resides in the host including memory request initiation, timing, scrubbing, sparing, and power management. The MB interface is responsible for memory requests to and from the local DIMM.

LRDIMM provides a high memory bandwidth, large capacity channel solution for DDR3 main memory systems. LRDIMM uses commodity DRAMs isolated from the channel behind the MB on the DIMM. The supported capacity exceeds 144 devices per channel (depending on channel and individual system design) and total memory capacity scales with DRAM bit density.



Feature	Application
▪ Fully compliant with JEDEC DDR3 Memory Buffer specification ▪ Speed up to DDR3-2133, DDR3L-1866 and DDR3U-1600 ▪ Registering and 1:2 redriving DDR3 command, address and parts of control buses ▪ Bidirectional retiming and 1:1 redriving of DDR3 data (DQ) signals ▪ Regeneration of data strobe (DQS) signals from input clock ▪ Generating clocks for DRAMs with a PVT stable phase relation to the input clock and redriven command, address and control signals ▪ Octal physical ranks supported ▪ x4 and x8 DRAM devices supported ▪ SMBus for read/write access to control registers ▪ On-die temperature sensor, accessible over SMBus ▪ Capability to supply reference voltage source for DRAMs ▪ Support for personality bytes ▪ Ultra Low power consumption ▪ 1.5V, 1.35V and 1.25V VDD ▪ Green package: 588-ball FBGA ▪ Command/Address Processing – Control word write procedure – Parity checking on command/address (CA) signals – Input bus termination (IBT) of the CA signals – CKE power management and clock stopped power-down mode – Dual frequency operation – Soft CKE mode – Refresh stagger supported – Re-generation of ODT for DRAM interface – Rank multiplication modes – Address/command/control net pre-launch and post-launch – 4 independent CKE outputs for DRAM – 8 independent chip select (CS) outputs for DRAM – Normal (300-1066MHz) and test mode (70-300MHz) frequencies – Programmable driver characteristics for DRAM interface – Weak drive mode of CA signals to save power – DRAM address inversion and MRS 3T timing mode ▪ Data Processing – One bidirectional data and data strobe DRAM interface – One bidirectional data and data strobe memory controller interface – 72 data and 18 differential data strobe signals – FIFOs for decoupling controller and DRAM interface time domains – Two timing modes for controller interface: minimum latency and minimum skew – Standard DDR3 DRAM requirements for the controller interface I/Os – Optimized low power I/Os for the DRAM interface – Write leveling support for the controller interface – On-chip calibration engine for DRAM interface read/write leveling and DQ/DQS relation ▪ DFX Features – Transparent mode – Memory BIST – Voltage margin test – Error injection	