

MICRON

MT4C4001

T-46-23-17

DRAM

1MEG x 4 DRAM

FAST PAGE MODE

DRAM

FEATURES

- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, and HIDDEN
- Optional Fast Page Mode access cycle

OPTIONS

MARKING

- Timing

80ns access	- 8
100ns access	-10
120ns access	-12
- Packages

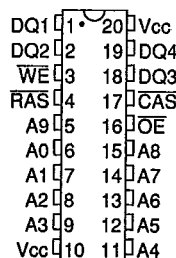
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

GENERAL DESCRIPTION

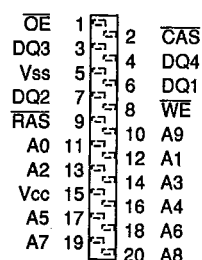
The MT4C4001 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), $\overline{\text{Q}}$ is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains low (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

PIN ASSIGNMENT (Top View)

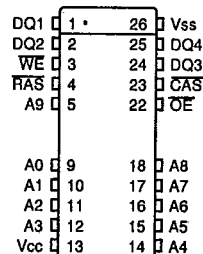
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



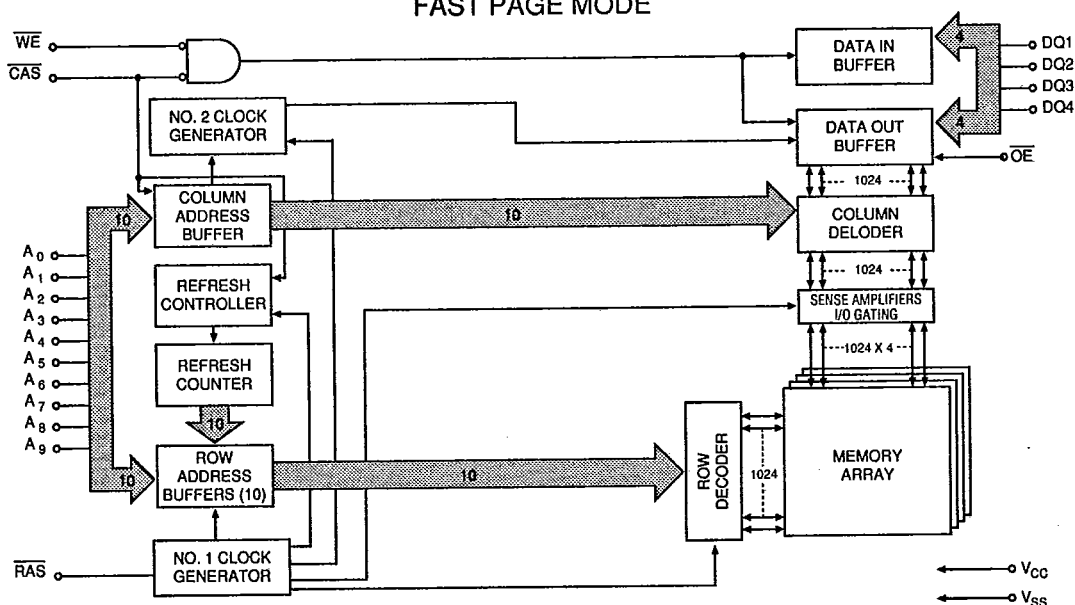
NOTE: packaging information to be determined

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{\text{RAS}}$ followed by a column address strobed in by $\overline{\text{CAS}}$. By holding $\overline{\text{RAS}}$ LOW, $\overline{\text{CAS}}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the PAGE MODE operation.

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**FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE****TRUTH TABLE**

Function	RAS	CAS	WE	Addresses		
				tR	tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss -1.0V to +7.0V
 Operating Temperature, T_A(Ambient) 0°C to +70°C
 Storage Temperature (Ceramic) -65°C to +150°C
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1 Watt
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DRAM**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V _{IN} ≤ 6.5V, all other pins not under test = 0 volts)	I _I	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High voltage (I _{OUT} = -5mA) Output Low voltage (I _{OUT} = 4.2mA)	V _{OH} V _{OL}	2.4	0.4	V V	

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-8	-10	-12		
OPERATING CURRENT Average power supply operating current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current (R _{AS} = C _{AS} = V _{IH})	I _{CC2}	3	2	2	mA	
R _{AS} ONLY REFRESH CURRENT Average power supply current, R _{AS} ONLY mode (R _{AS} Cycling, C _{AS} =V _{IH} : t _{RC} = t _{RC} (MIN))	I _{CC3}	100	85	60	mA	3
FAST PAGE MODE CURRENT Average power supply current, Fast Page Mode (R _{AS} = V _{IL} , C _{AS} , Address Cycling: t _{PC} = t _{PC} (MIN))	I _{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current (R _{AS} = C _{AS} = V _{CC} -0.2V)	I _{CC5}	1	1	1	mA	
C _{AS} -BEFORE-R _{AS} REFRESH CURRENT Average power supply current, C _{AS} -BEFORE-R _{AS} Mode (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC6}	100	85	60	mA	3

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C _{I2}		7	pF	2
Input/Output Capacitance: DQ	C _{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	t _{RC}	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t _{RWC}	205		245		295		ns	
PAGE-MODE READ or WRITE cycle time	t _{PC}	50		60		70		ns	
Access time from RAS	t _{RAC}		80		100		120	ns	14
Access time from CAS	t _{CAC}		20		25		35	ns	15
Output Enable	t _{OE}		25		25		30	ns	
Access time from column address	t _{AA}		40		50		60	ns	
Access time from CAS precharge	t _{CPA}		45		55		65	ns	
RAS pulse width	t _{RAS}	80	10,000	100	10,000	120	10,000	ns	
RAS pulse width (PAGE MODE)	t _{RASP}	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	t _{RSH}	20		25		35		ns	
RAS precharge time	t _{RP}	70		80		90		ns	
CAS pulse width	t _{CAS}	20	10,000	25	10,000	35	10,000	ns	
CAS hold time	t _{CSH}	80		100		120		ns	
CAS precharge time	t _{CPN}	15		15		20		ns	16
CAS precharge time (PAGE MODE)	t _{CP}	15	25	15	25	15	25	ns	
RAS to CAS delay time	t _{RCD}	20	60	25	75	35	85	ns	17
CAS to RAS precharge time	t _{CRP}	10		10		10		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	12		15		20		ns	
RAS to column address delay time	t _{RAD}	15	40	20	50	30		ns	18
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	15		20		25		ns	
Column address hold time (referenced to RAS)	t _{AR}	60		75		90		ns	
Column address to RAS lead time	t _{RAL}	40		50		60		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time (referenced to CAS)	t _{RCH}	0		0		0		ns	19
Read command hold time (referenced to RAS)	t _{RRH}	0		0		0		ns	19
CAS to output in low-Z	t _{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t _{OFF}	0	20	0	25	0	25	ns	20
Output Disable	t _{OD}		25		25	30	25	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
WE command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	
FAST PAGE MODE READ-MODIFY-WRITE cycle time	t_{PRWC}	100		115		140		ns	
Write command hold time (referenced to RAS)	t_{WCR}	60		75		90		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to RAS lead time	t_{RWL}	20		25		30		ns	
Write command to CAS lead time	t_{CWL}	20		25		30		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		20		25		ns	22
Data-in hold time (referenced to RAS)	t_{DHR}	60		75		90		ns	
RAS to WE delay time	t_{RWD}	110		135		160		ns	21
Column address to WE delay time	t_{AWD}	70		85		100		ns	21
CAS to WE delay time	t_{CWD}	25		25		75		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t_{REF}		16		16		16	ms	
RAS to CAS Precharge time	t_{RPC}	0		0		0		ns	
CAS set-up time (CAS-BEFORE-RAS refresh)	t_{CSR}	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	t_{CHR}	20		20		30		ns	5

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leq T_A \leq 70^{\circ}C$) is assured.
7. An initial pause of 100 μ s is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $t_{RCD} < t_{RCD}^{(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD}^{(max)}$.
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{RCD}^{(max)}$ limit ensures that $t_{RAC}^{(max)}$ can be met. $t_{RCD}^{(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}^{(max)}$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD}^{(max)}$ limit ensures that $t_{RCD}^{(max)}$ can be met. $t_{RAD}^{(max)}$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}^{(max)}$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF}^{(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS}^{(min)}$, the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}^{(min)}$, $t_{AWD} \geq t_{AWD}^{(min)}$ and $t_{CWD} \geq t_{CWD}^{(min)}$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.

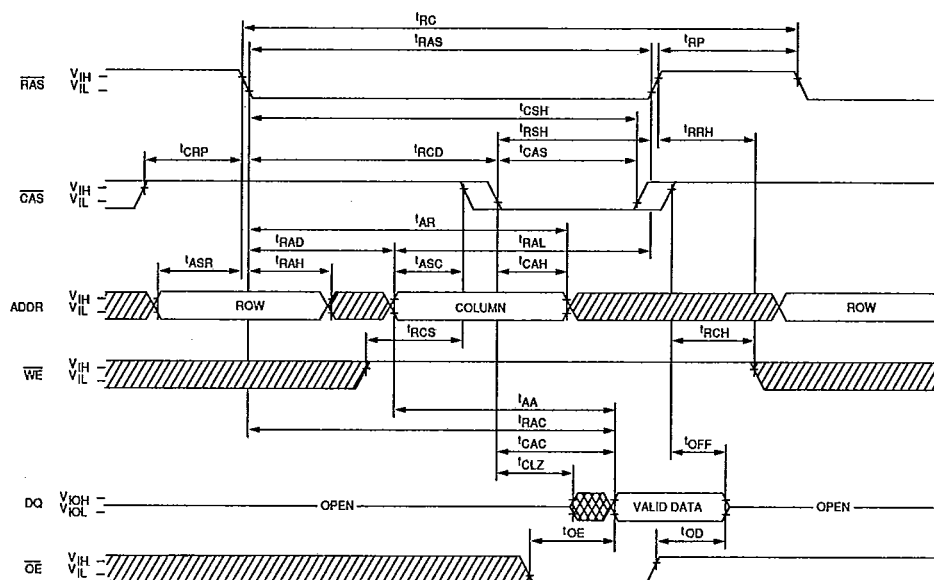
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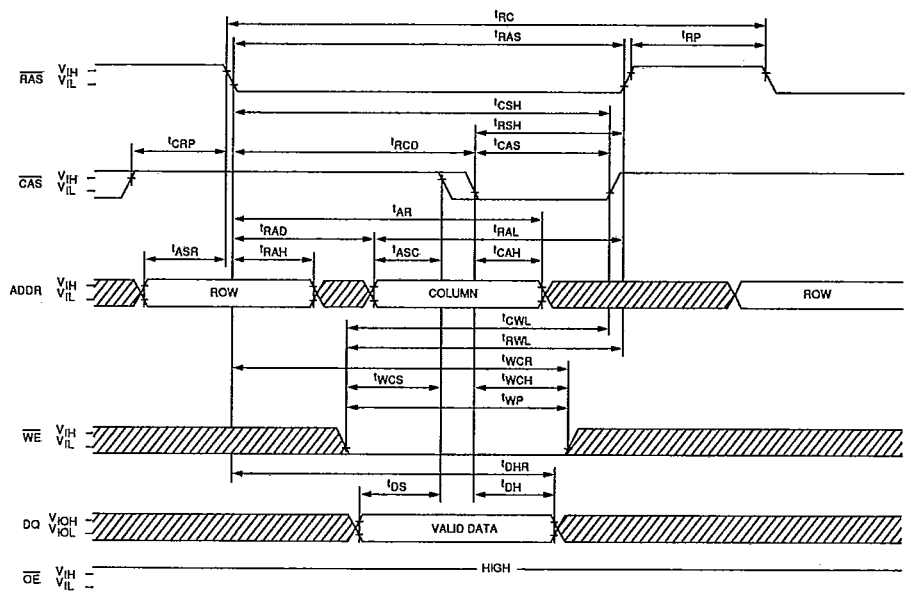
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READ CYCLE



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EARLY-WRITE CYCLE

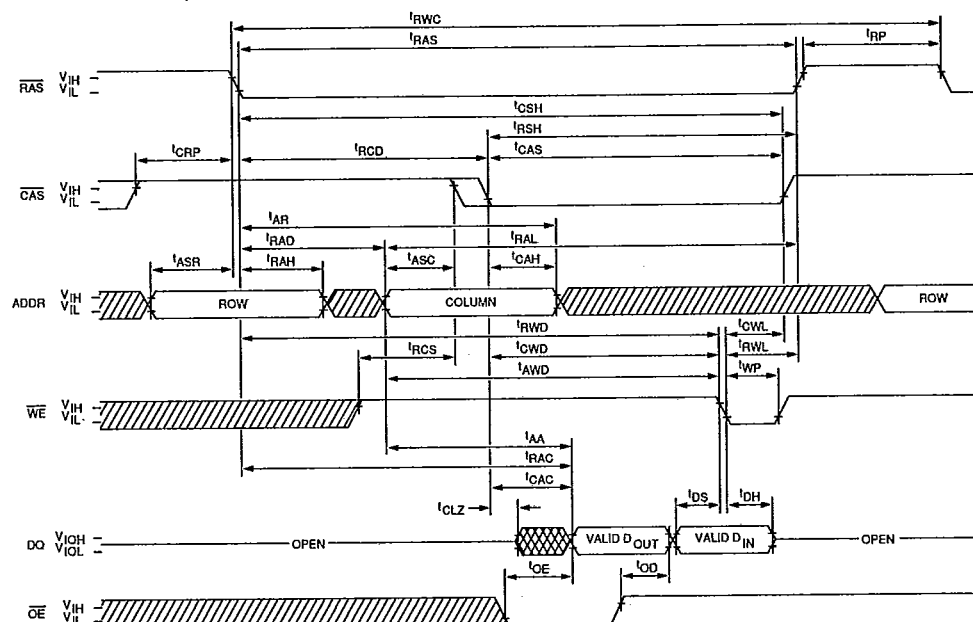


DON'T CARE
 UNDEFINED

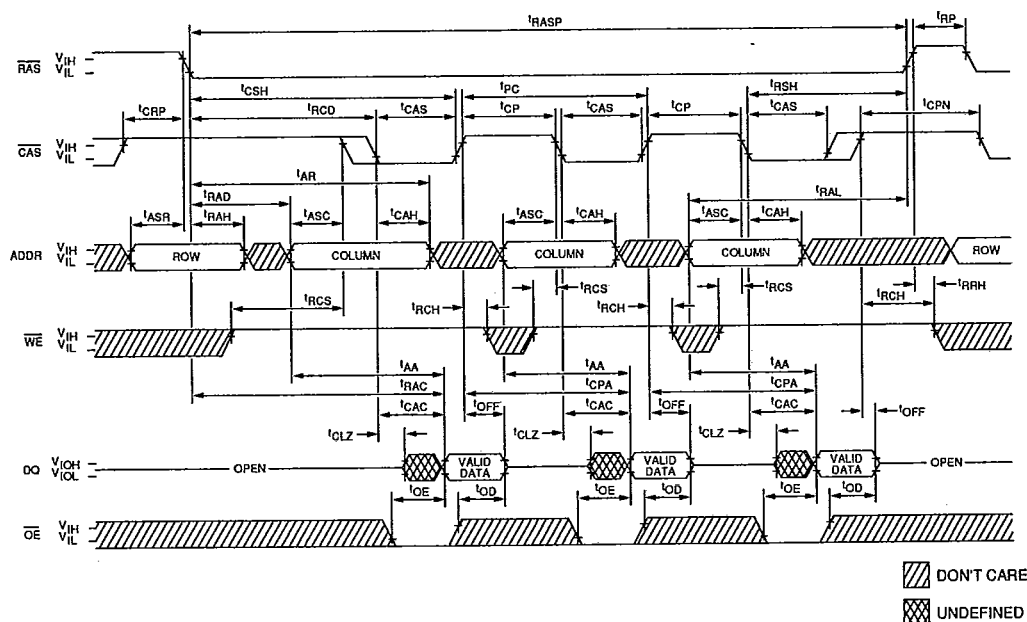
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READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE



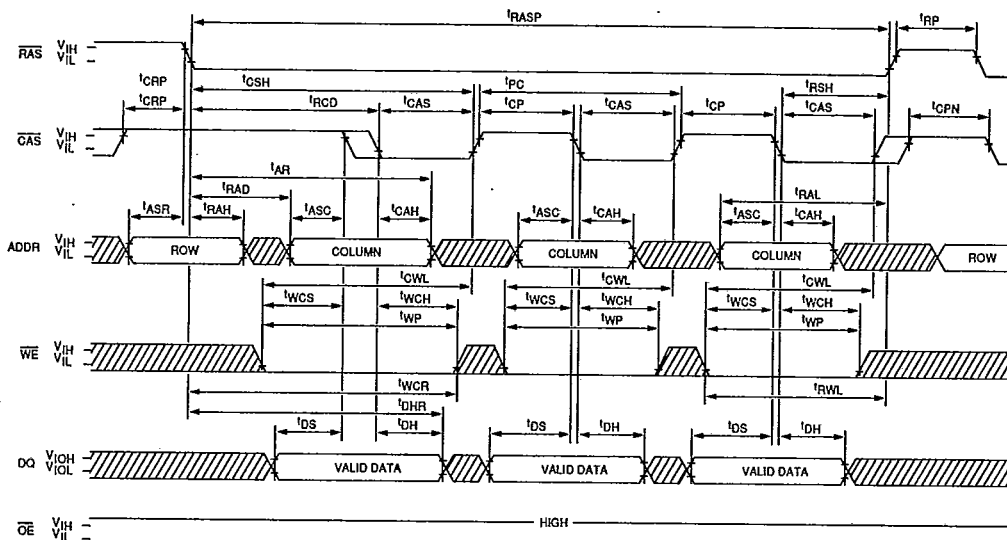
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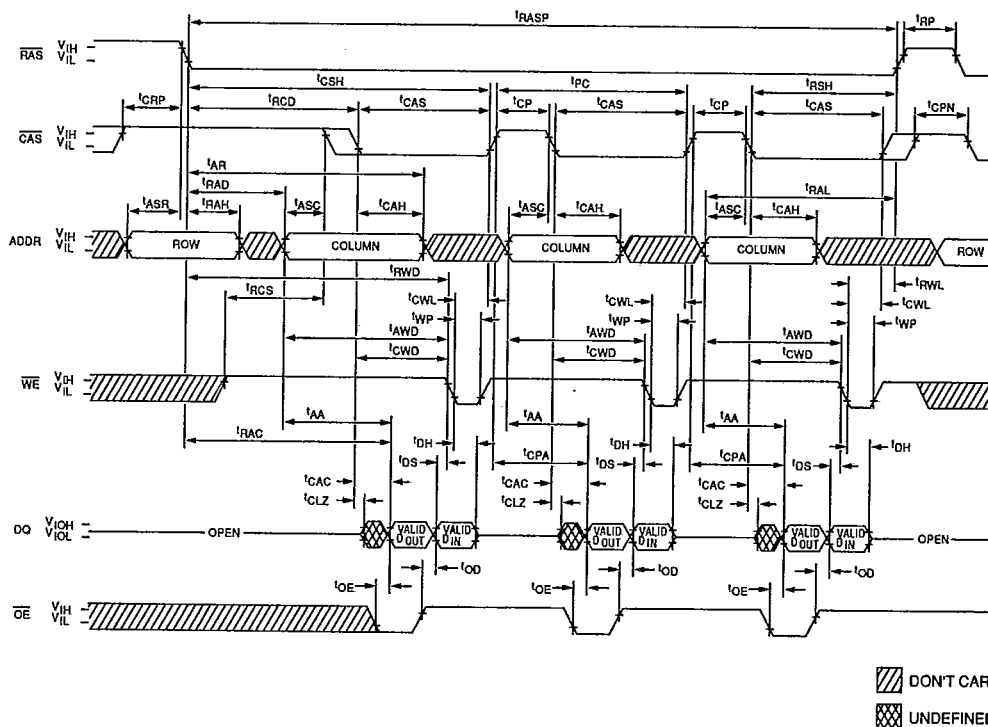
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PAGE-MODE EARLY-WRITE CYCLE



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PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

▨ DON'T CARE
▩ UNDEFINED

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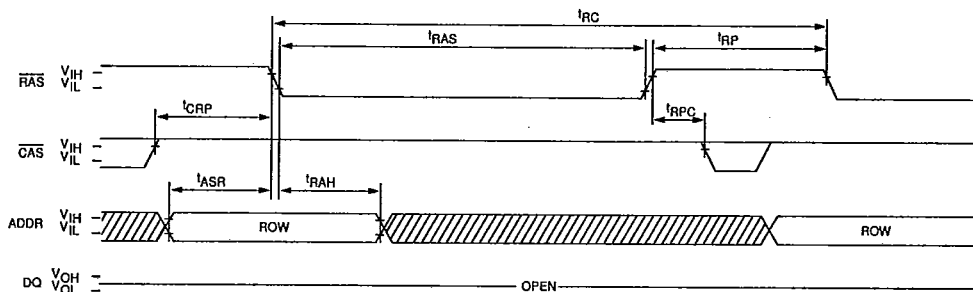
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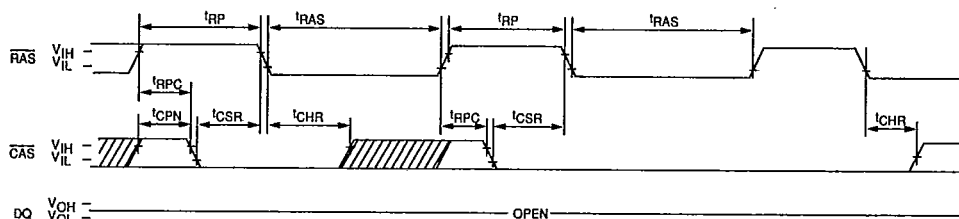
RAS ONLY REFRESH CYCLE

(ADDR = $A_0 - A_9$; $\overline{WE}$ = DON'T CARE.)



CAS-BEFORE-RAS REFRESH CYCLE

($A_0 - A_9$, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW)²⁴

