Rockwell

R144EFXL Low Power 14400 bps MONOFAX® Modem

INTRODUCTION

The Rockwell R144EFXL MONOFAX modem is a synchronous 14400 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires only a single +5VDC power supply. The modem is housed in a single VLSI device package.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the requirements specified in CCITT recommendations V.33, V.17, V.29, V.27 ter, V.21 Channel 2 (FSK), T.4, and T.3, and meets the binary signaling requirements of T.30.

The modem can operate at 14400, 12000, 9600, 7200, 4800, 2400, or 300 bps. The modem supports the V.17 signalling rates of 14400, 12000, 9600, and 7200 bps using trellis-coded modulation (TCM). In addition, the modem supports V.27 ter and V.17 short trains.

The modem can also perform HDLC framing according to T.30 at 14400, 12000, 9600, 7200, 4800, 2400, or 300 bps.

An FSK flag pattern (7E) detector facilitates FSK detection in the high speed receiver.

The voice mode allows the host computer (DTE) to transmit and receive audio signals and messages.

The modem includes a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 (FSK) receiver. The three programmable tone detectors also operate concurrently with the voice mode receiver.

General purpose input/output (GPIO) and general purpose input (GPI) pins are available for host assignment in the 100-pin PQFP.

The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.

The modem is available in either a 100-pin plastic quad flat pack (PQFP) or a 64-pin quad in-line package (QUIP). The packages are shown in Figure 1. The general modem interface is illustrated in Figure 2.

Additional modem information is described in the R144EFXL MONOFAX Modem Designer's Guide (Order No. 895).

FEATURES

- Group 3 facsimile transmission/reception
  - CCITT V.33, V.17, V.29, V.27 ter, V.21 Channel 2 (FSK), T.4, and T.30
  - HDLC Framing at all speeds
- Group 2 facsimile transmission/reception
  - CCITT T.3
  - External clock tracking
- V.27 ter short train
- V.29 short train
- Concurrent DTMF, FSK, and tone reception
  - Concurrent DTMF reception, FSK flag pattern (7E) detection, and tone detection
- FSK flag pattern detect during high speed reception
- Voice mode transmission/reception
- 2-wire half-duplex
- Programmable transmit level: 0 to –15 dBm
- Programmable transmit analog attenuation: 0 dB to 14 dB in 2 dB steps
- Receive dynamic range: 0 to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - Allows telephone line quality monitoring
- Compromise equalization
  - Automatic adaptive and fixed digital
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption:
  - Operating mode: 270 mW (typical)
  - Sleep mode: 17 mW (typical)
- Single +5VDC power supply
- Single Package
  - 100-pin PQFP or 64-pin QUIP
- Hardware compatible with the R96DFXL MONOFAX modem
- Software compatible with all MONOFAX modems

Document No. 29200N90 | **Data Sheet (Preliminary)** | **Order No. MD90 October 1992**

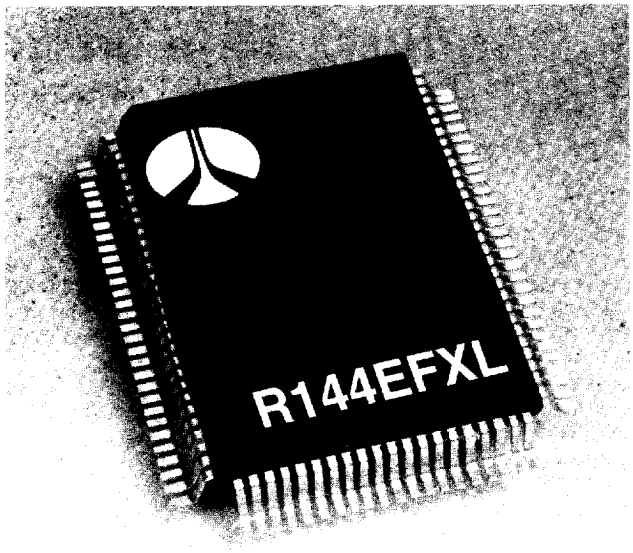

Figure 1. R144EFXL MONOFAX Modem

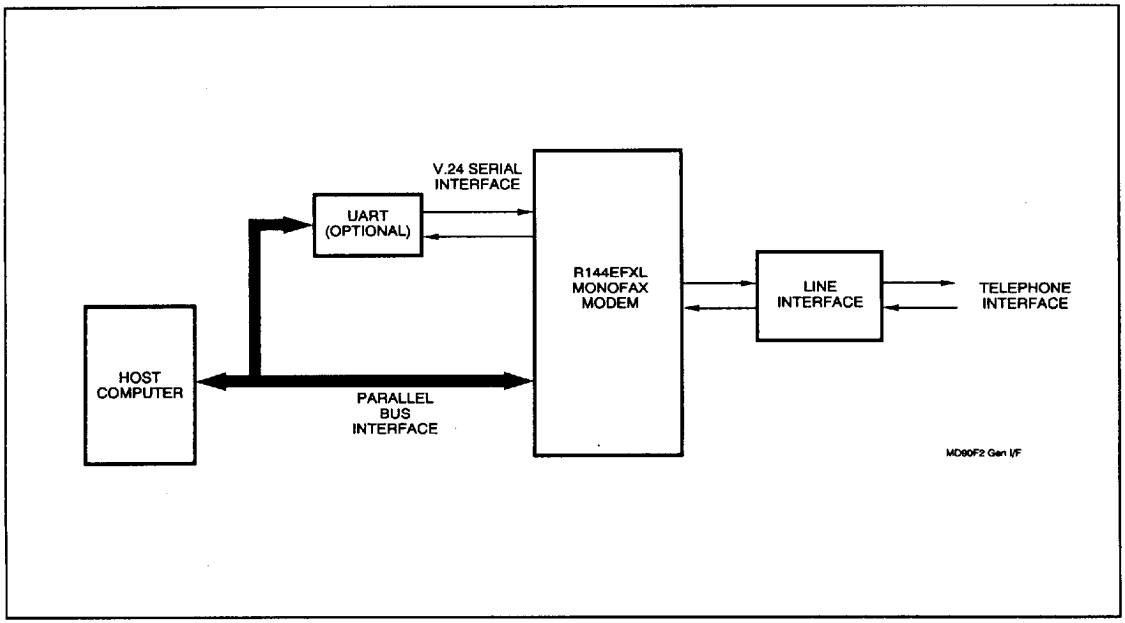

Figure 2. R144EFXL MONOFAX Modem General Interface

TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.33, V.17, V.29, V.27 ter, V.21 Channel 2, and T.3.

Automatic Adaptive Equalizer

An adaptive equalizer in V.33, V.17, V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Fixed Digital Cable Compromise Equalizer

Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive and transmit data path. The gain and delay response curves are shown in Figure 3.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ± 0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.33/V.17 14400	TCM	1700 or 1800	14400	2400	6	128
V.33/V.17 12000	TCM	1700 or 1800	12000	2400	5	64
V.17 9600	TCM	1700 or 1800	9600	2400	4	32
V.17 7200	TCM	1700 or 1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650,1850	300	300	1	–
T.3 (Group2)	VSAMPM	2100	–	–	–	–

Note:

1. Modulation legend:
   - QAM Quadrature Amplitude Modulation
   - DPSK Differential Phase Shift Keying
   - FSK Frequency Shift Keying
   - TCM Trellis Coded Modulation
   - VSAMPM Vestigal Sideband Amplitude Modulation - Phase Modulation

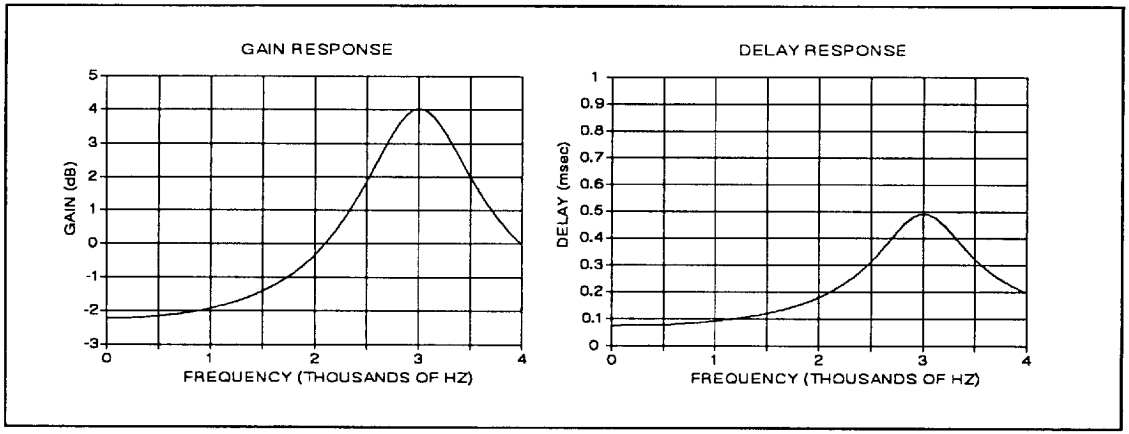

Figure 3. Digital Cable Equalizer Frequency Response

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter energy levels in the 4 – 50 kHz frequency range are below –55.0 dBm.

Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 2.

Turn-off Sequence

Transmitter turn-off sequence times are shown in Table 3.

Transmit Level

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Additionally, the modem can be programmed to attenuate the transmit output level from 0 dB to -14 dB in the analog section in steps of 2 dB using the TXLOSS1 - TXLOSS3 input pins (see Table 11 for encoding).

Table 2. Turn-On Sequence Times

Configuration	$\overline{RTS}$ On to $\overline{CTS}$ On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.33/V.17	1393 ms	1600 ms
V.17 Short Train	142 ms	349 ms
V.29 Long Train	253 ms	441 ms
V.29 Short Train	75 ms	282 ms
V.27 ter 4800 bps Long Train	708 ms	915 ms
V.27 ter 4800 bps Short Train	50 ms	257 ms
V.27 ter 2400 bps Long Train	943 ms	1150 ms
V.27 ter 2400 bps Short Train	67 ms	274 ms
V.21 Channel 2 300 bps	≤ 14 ms	≤ 14 ms
Group 2	≤ 400 ms	≤ 400 ms

Table 3. Turn-Off Sequence Times

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.33/V.17	13.3 ms	20 ms	33.3 ms
V.17 Short Train	13.3 ms	20 ms	33.3 ms
V.29 Long and Short Train	5 ms	20 ms	25 ms
V.27 ter 4800 bps Long Train	7 ms	20 ms	27 ms
V.27 ter 4800 bps Short Train	7 ms	20 ms	27 ms
V.27 ter 2400 bps Long Train	10 ms	20 ms	30 ms
V.27 ter 2400 bps Short Train	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms

Notes:

1. In parallel data mode, the turn-off sequence may be extended by 8 bit times.
2. In HDLC mode, the turn-off sequence may be extended by more than 8 bit times.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.33, V.17, V.29, or V.27 ter recommendations, depending on the selected configuration.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable Received Line Signal Detector ($\overline{RLSD}$) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The $\overline{RLSD}$ threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

Receiver Timing

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever $\overline{RLSD}$ is off.

Tone Detectors

Tone detectors 1 and 2 operate in all non-high speed receive modes. Tone detector 3 operates in all receive modes. The tone detectors can also operate as one 12th order filter in non-high speed receive modes.

The filter coefficients of each filter are host programmable in RAM. The output of the tone detector filter goes to an energy detector.

Voice Mode

The voice mode enables the host to efficiently transmit and receive audio signals and messages. In this mode, the host can directly access modem analog-to-digital (A/D) and digital-to-analog (D/A) converters. Incoming analog voice signals can then be converted to digital format and digital signals can be converted to analog voice output.

Sleep Mode

The modem can be put into low power Sleep mode by writing 0 into the Sleep Mode Enable DSP RAM parameter (see No. 53 in Table 13). When this occurs, the modem XTLI pin is pulled down internally with 10K - 30K ohms impedance to disable the internal oscillator. All of the oscillator outputs (e.g., XCLK, YCLK, DCLK, etc.) are disabled and the GPIO lines pulled up to +5VD with about 50K ohms impedance. The power consumption will drop to about 17 mW if a crystal is used or to about 33 mW if an external oscillator is used (since XTLI and XTLO are still active). In either case, the XCLK and YCLK outputs are disabled, therefore, the host cannot use either clock in the Sleep mode. Return to normal operation is initiated when the Power-On-Reset Input ($\overline{\text{PORI}}$) signal is asserted or the host writes to any modem interface memory location. The modem will perform self-test, configure itself to power-on-reset default conditions, and be ready for normal use within 30 ms.

General Specifications

The modem power and environmental requirements are shown in Tables 4 and 5, respectively.

Table 4. Power Requirements

Voltage	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+5 VDC ±5%	54 mA	60 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 μV peak.

Table 5. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32 °F to 158°F)
Storage	–55°C to 125°C (–67°F to 257°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

HARDWARE INTERFACE SIGNALS

The modem functional hardware interface signals are shown in Figure 4. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for EIA-232-D) is called active low and is represented by a small circle at the signal point. Active low signals are overscored (e.g., $\overline{POR}$).

Edge-triggered clocks are indicated by a small triangle (e.g., DCLK).

Open-collector (open-source or open-drain) outputs are denoted by a small half circle (e.g., signal $\overline{IRQ}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The pin assignments for the 64-pin QUIP are listed by pin number in Table 6 and are shown in Figure 5.

The pin assignments for the 100-pin PQFP are listed by pin number in Table 7 and are shown in Figure 6.

The hardware interconnect signals are listed by functional group in Table 8. The digital signal interface characteristics are defined in Table 9. The analog signal interface characteristics are defined in Table 10. The hardware interface signals are defined in Table 11.

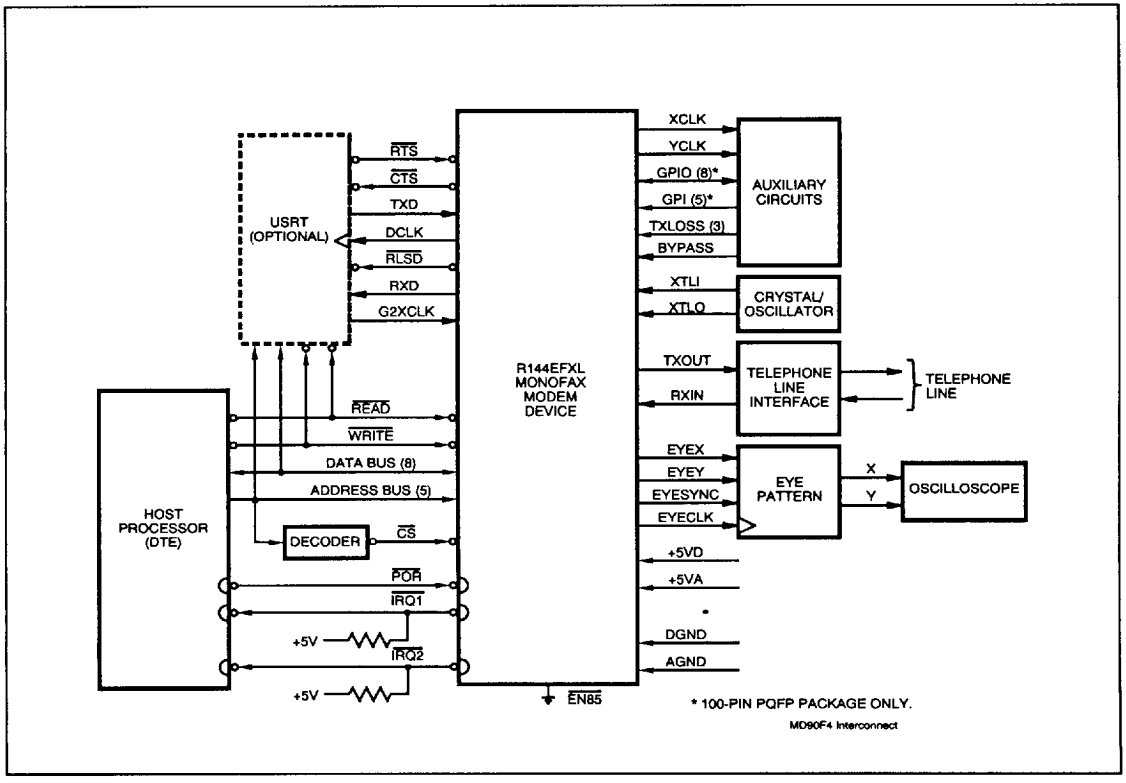

Figure 4. Modem Functional Interconnect Diagram

Table 6. Pin Signals - 64-Pin QUIP

Pin No.	Signal Name	I/O Type
1	RS1	IA
2	RS0	IA
3	RTS	IA
4	EN85	R
5	PORI	ID
6	XTLI	R
7	XTLO	R
8	XCLK	OD
9	YCLK	OD
10	+5VD1	PWR
11	IRQ2/DCLKI	OC/R
12	G2XCLK	IA
13	0VD2	GND
14	CTS	OA
15	TXD	IA
16	DCLK	OA
17	EYESYNC	OA
18	EYECLK	OA
19	EYEX	OA
20	ADIN	R
21	DAOUT	R
22	NC	
23	NC	
24	+5VD2	PWR
25	0VD1	GND
26	SWGAINI	R
27	ECLKIN1	R
28	SYNCIN1	R
29	DAIN	R
30	ADOUT	R
31	BYPASS	IC
32	RCVI	R
33	TXLOSS3	IC
34	TXLOSS2	IC
35	TXLOSS1	IC
36	TXOUT	AA
37	RXIN	AB
38	+5VA	PWR
39	0VA	GND
40	AGD	R
41	AOUT	R
42	RAMPIN	R
43	0VD2	GND
44	EYEY	OA
45	RXD	OA
46	RLSD	OA
47	RCVO	R
48	SWGAINO	R
49	0VD2	GND
50	D7	IA/OB
51	D6	IA/OB
52	D5	IA/OB
53	D4	IA/OB
54	D3	IA/OB
55	D2	IA/OB
56	D1	IA/OB
57	D0	IA/OB
58	IRQ1	OC
59	WRITE-R/W	IA
60	CS	IA
61	READ-φ2	IA
62	RS4	IA
63	RS3	IA
64	RS2	IA

Notes:

1. NC = No connection, leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 9;
   Analog signals: see Table 11.
3. R = Required overhead connection; no connection to host equipment.

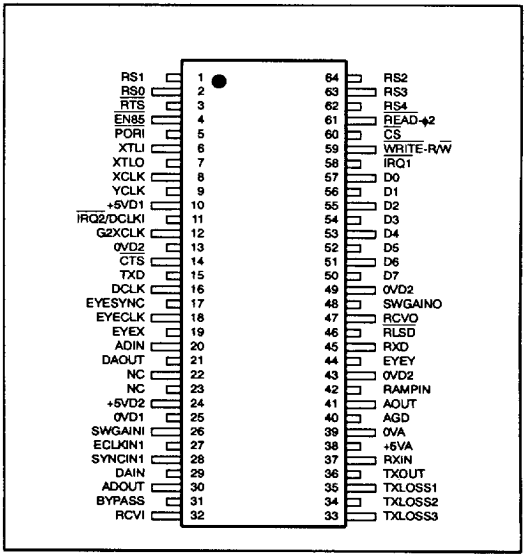

Figure 5. Pin Signals - 64-Pin QUIP

Table 7. Pin Signals - 100-Pin PQFP

Pin No.	Signal Name	I/O Type
1	GP03	IA/OB
2	GP04	IA/OB
3	GP05	IA/OB
4	GP06	IA/OB
5	GP07	IA/OB
6	0VD2	GND
7	0VD2	GND
8	D7	IA/OB
9	D6	IA/OB
10	D5	IA/OB
11	D4	IA/OB
12	D3	IA/OB
13	D2	IA/OB
14	D1	IA/OB
15	D0	IA/OB
16	0VD2	GND
17	0VA	GND
18	RAMPIN	R
19	NC	
20	NC	
21	0VA	GND
22	+5VD2	PWR
23	0VD1	GND
24	SWGAINI	R
25	ECLKIN1	R
26	SYNCIN1	R
27	NC	
28	NC	
29	NC	
30	0VA	GND
31	NC	
32	NC	
33	NC	
34	DAIN	R
35	ADOUT	R
36	BYPASS	IC
37	RCVI	R
38	TXLOSS3	IC
39	TXLOSS2	IC
40	TXLOSS1	IC
41	NC	
42	NC	
43	0VA	GND
44	TXOUT	AA
45	RXIN	AB
46	+5VA	PWR
47	0VA	GND
48	AGD	R
49	AOUT	R
50	0VD1	GND
51	NC	
52	IRQ1	OC
53	WRITE-R/W	IA
54	CS	IA
55	READ-ϕ2	IA
56	RS4	IA
57	RS3	IA
58	RS2	IA
59	RS1	IA
60	RS0	IA
61	GP13	IA/OB
62	+5VD1	PWR
63	GP11	IA/OB
64	RTS	IA
65	EN85	R
66	0VD2	GND
67	PORI	ID
68	XTLI	R
69	XTLO	R
70	XCLK	OD
71	YCLK	OD
72	+5VD1	PWR
73	IRQ2/DCLKI	OC/R
74	G2XCLK	IA
75	GP16	IA/OB

Table 7. Pin Signals - 100-Pin PQFP (Cont'd)

Pin No.	Signal Name	I/O Type
76	GP17	IA/OB
77	0VD2	GND
78	CTS	OA
79	TXD	IA
80	0VD2	GND
81	0VD2	GND
82	DCLK	OA
83	EYESYNC	OA
84	EYECLKX	OA
85	EYECLK	OA
86	EYEX	OA
87	ADIN	R
88	DAOUT	R
89	0VD2	GND
90	EYEY	OA
91	GP21	IA/OB
92	0VD2	GND
93	GP20	IA/OB
94	GP19	IA/OB
95	RXD	OA
96	RLSD	OA
97	0VD2	GND
98	RCVO	R
99	SWGAINO	R
100	GP02	IA/OB

Notes:

1. NC = No connection; leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 9;
   Analog signals: see Table 11.
3. R = Required modem inter-connection; no connection to host equipment.

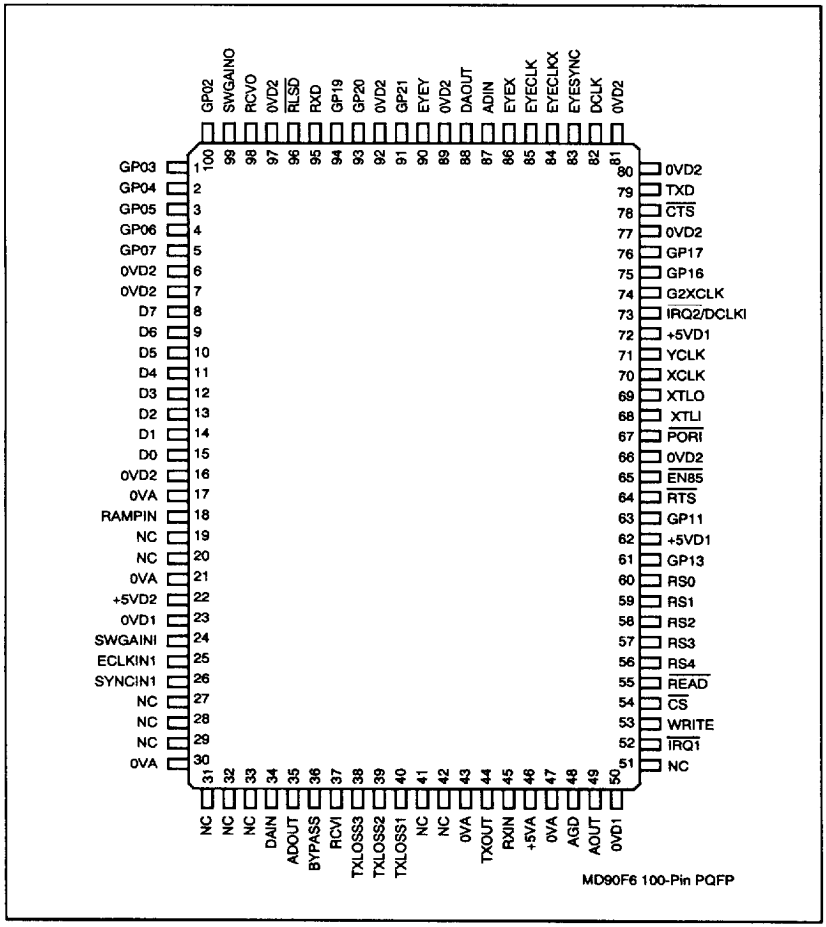

Figure 6. Pin Signals - 100-Pin PQFP

Table 8. Modem Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORI	ID	Power-On-Reset Input
+5VDx	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
0VDx	GND	Connect to Digital Ground
0VA	GND	Connect to Analog 0V Ground
AGD	R	+2.5 V Analog Ground
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
CS	IA	Chip Select
READ-φ2	IA	Read Enable (808X), φ2 Clock (65XX)
WRITE-R/W	IA	Write Enable (808X), R/W (65XX)
IRQ1, IRQ2	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
RTS	IA	Request to Send
CTS	OA	Clear to Send
RLSD	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
G2XCLK	IA	Group 2 External Transmit and Receive Data Clock
Auxiliary Signals		
BYPASS	IC	Receiver Highpass Filter Bypass Enable
TXLOSS1	IC	2 dB of Analog Transmit Level Attenuation
TXLOSS2	IC	4 dB of Analog Transmit Level Attenuation
TXLOSS3	IC	8 dB of Analog Transmit Level Attenuation
XCLK	OD	19 MHz Output
YCLK	OD	9.5 MHz Output
EN85	IA	Enable 8085 Bus
GPx	IA/OB	General Purpose Input/Output[3]

Table 8. Modem Hardware Interface Signals (Cont'd)

Name	Type[1]	Description
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock (576 kHz)
EYESYNC	OA	Serial Eye Pattern Strobe (9600 Hz)
Modem Interconnect		
DCLKI	R	May connect to DCLK if IRQ2 is not used.
ECLKIN1	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
SWGAINI	R	Connect to SWGAINO
SWGAINO	R	Connect to SWGAINI
RAMPIN	R	Receiver Amplifier Input
AOUT	R	Smoothing Filter Output

Notes:

1. Digital signals are described in Table 9. Analog signals are described in Table 11.
2. R = Required overhead connection; no connection to host equipment.
3. 100-pin PQFP only.

Table 9. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type IC and ID		0.8(V_{CC})	–	V_{CC}		
Input High Current	I_{IH}				µA	V_{CC} = 5.25 V, V_{IN} = 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}					Vdc
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (VCC)		
Input Low Current	I_{IL}	–	–	–400	µA	V_{CC} = 5.25 V
Type IB and IC						
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5 V, V_{CC} = 5.25 V
Types IA and ID						
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OE		2.4	–	–		I_{LOAD} = –40 µA
Output High Current	I_{OH}	–	–	–0.1	mA	
Type OD						
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OE		–		0.4		I_{LOAD} = 0.4 mA
Output Low Current	I_{OL}	–	–	100	µA	
Type OD						
Output Leakage Current	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock
Power Dissipation	P_D	–				VCC = 5.0 V @ 25°C for P_D typ.;
Normal Mode			270	300	mW	VCC = 5.25 V @ 0°C for P_D max.
Sleep Mode (External Crystal)			17	19	mW	
Sleep Mode (External Oscillator)			33	36	mW	

Table 10. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +5VD +0.5	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog inputs	V_{IN}	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Z State	V_{HZ}	-0.5 to +5VD + 0.5	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V

Table 11. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	R R	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 38.000530 MHz crystal and two capacitors , or a square wave generator/sine wave oscillator.
$\overline{\text{PORI}}$	ID	**Power-On-Reset Input.** After application of +5V power to the modem, $\overline{\text{PORI}}$ must be held low for at least 5 ms after the +5V power reaches operating range. The modem is ready to use 30 ms after the low-to-high transition of $\overline{\text{PORI}}$. The POR sequence initializes the modem interface memory (Table 12) to default values.
+5VD1 +5VD2	PWR	**+ 5V Digital Supply.** +5VD1 and +5VD2 must be connected to +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 5%.
0VD1 0VD2	GND	**Digital Ground.** 0VD1 and 0VD2 must be connected to digital ground.
0VA	GND	**Analog Ground.** 0VA must be connected to analog ground.
AGND	R	**2.5 V Analog Ground Output.** This is used as an internal ground for the modem.
		MICROPROCESSOR BUS INTERFACE Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. Note that the modem should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 211 ns from a preceding write cycle.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable ($\overline{\text{READ}}$-ϕ2) and Write Enable (WRITE-R/$\overline{\text{W}}$) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0-A4. When selected by $\overline{\text{CS}}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
$\overline{\text{CS}}$	IA	**Chip Select.** The active low $\overline{\text{CS}}$ input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus. The $\overline{\text{CS}}$ input line is typically connected to address line A5 through a decoder.

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{\text{READ}}$–φ2 $\overline{\text{WRITE}}$–R/$\overline{\text{W}}$	IA IA	**Read Enable–φ2.** **Write Enable–R/$\overline{\text{W}}$.** When $\overline{\text{EN85}}$ is low (8085 bus selected), reading or writing is controlled by the host pulsing either $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ input low, respectively, during the microprocessor bus access cycle. The read/write timing (corrsponding to the waveforms shown in Figure 2-3 of the R144EFXL Designer's Guide) is:
$\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$	OC, OC	**Interrupt Request.** $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ interrupt request outputs may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. (The term, "$\overline{\text{IRQ}}$", refers to both the $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ output lines in the following discussion.)The $\overline{\text{IRQ}}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of $\overline{\text{IRQ}}$ is optional depending upon modem application. The $\overline{\text{IRQ}}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{\text{IRQ}}$ output can be wire-ORed with other $\overline{\text{IRQ}}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{\text{IRQ}}$ lines have returned high). Because of the open-drain structure of $\overline{\text{IRQ}}$, an external pull-up resistor to +5V is required at some point on the $\overline{\text{IRQ}}$ line. The resistor value should be small enough to pull the $\overline{\text{IRQ}}$ line high when all $\overline{\text{IRQ}}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{\text{IRQ}}$ output is used, a resistor value of 5.6K ohms 20%, 0.25 W, is sufficient.
		V.24 SERIAL INTERFACE These pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (PDM bit = 0), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (PDM bit = 1).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in parallel data mode.
$\overline{\text{RTS}}$	IA	**Request to Send.** The active low $\overline{\text{RTS}}$ input allows the modem to transmit data present at TXD in the serial data mode (PDM bit = 0), or in DBUFF in the parallel data mode (PDM bit = 1), when $\overline{\text{CTS}}$ becomes active. The $\overline{\text{RTS}}$ hardware control input is logically ORed with the RTSP bit (Table 12) by the modem to form the resultant control signal.

Parameter	Symbol	Min.	Max.	Units
$\overline{\text{CS}}$ Setup Time	TCS	0	–	ns
RSI Setup Time	TRS	10	–	ns
Data Access Time	TDA	–	45	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns
Phase 2 (φ2) Clock High	TP2CH	70	–	ns

Notes:
1. $\overline{\text{CS}}$ and $\overline{\text{READ}}$ must not both be active continuously.
2. A read or write operation following a write operation must be delayed by at least 2 YCLK cycles (211 ns).
3. A read or write operation following a read operation must be delayed by at least 1 YCLK cycle (105 ns).

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{\text{CTS}}$	OA	**Clear To Send.** $\overline{\text{CTS}}$ active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. $\overline{\text{CTS}}$ response times from $\overline{\text{RTS}}$ on are shown in Table 2. The $\overline{\text{CTS}}$ hardware status output parallels the operation of the CTSP bit (Table 12).
$\overline{\text{RLSD}}$	OA	**Received Line Signal Detector.** For V.33, V.17, V.29, and V.27 ter; $\overline{\text{RLSD}}$ goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the $\overline{\text{RLSD}}$ off-to-on response time is 804 baud times. The $\overline{\text{RLSD}}$ on-to-off time is 40 ± 5 ms for V.33/V.17, 35 ± 5 ms for V.29 or 11.6 ± 5 ms for V.27 ter. The $\overline{\text{RLSD}}$ on-to-off time ensures that all valid data bits have appeared on RXD. The $\overline{\text{RLSD}}$ programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a single mode-dependent synchronous data clock (DCLK) for USRT timing. The DCLK frequency is 14400, 12000, 9600, 7200, 4800, 2400, or 300 Hz (0.01%) with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK. The DCLK frequency tracks a 10368 Hz clock on G2XCLK input in Group 2 when G2CTK bit is a 1.
G2XCLK	IA	**Group 2 External Transmit and Receive Data Clock.** In Group 2, the modem will track an externally provided 10368 Hz clock on G2XCLK when the G2CTK bit = 1. G2XCLK may be connected to SYNCIN1 if the external clock is not used. (SeeDCLK.)
		AUXILIARY SIGNALS
$\overline{\text{EN85}}$	R	**Enable 85 Bus.** The $\overline{\text{EN85}}$ input selects the modem microprocessor bus compatibility. When $\overline{\text{EN85}}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$. When $\overline{\text{EN85}}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using $\phi 2$ and R/$\overline{\text{W}}$. In the 6500 configuration, the $\overline{\text{READ}}$ input becomes $\phi 2$ and the $\overline{\text{WRITE}}$ input becomes R/$\overline{\text{W}}$. This selection is performed only during initialization, i.e., when $\overline{\text{POR}}$ is asserted.
TXLOSS1 TXLOSS2 TXLOSS3	IC IC IC	**Analog Transmit Attentuation.** The host can cause the modem to attentuate the transmit analog output in steps of 2 dB from 0 dB to -14 dB by using the three encoded TXLOSSx inputs as follows: **TXLOSS3 / TXLOSS2 / TXLOSS1 / Attentuation (dB)** 0 / 0 / 0 / 0 0 / 0 / 1 / 2 0 / 1 / 0 / 4 0 / 1 / 1 / 6 1 / 0 / 0 / 8 1 / 0 / 1 / 10 1 / 1 / 0 / 12 1 / 1 / 1 / 14 The TXLOSSx lines may be connected directly to 0V or +5V. With the 100-pin PQFP, the TXLOSSx lines may be connected to three GPIO lines used as outputs to select the attentuation under host program control.
XCLK	OD	**XCLK Output.** XCLK is a 19 MHz square wave output derived from XTLI (XTLI divided by 2).
YCLK	OD	**YCLK Output.** YCLK is a 9.5 MHz square wave output derived from XTLI (XTLI divided by 4).
BYPASS	IC	**Receiver Highpass Filter Bypass Enable.** This input enables (high) or disables bypass of the receiver highpass filter of the received analog input signal. For normal operation, this pin should be connected to 0VA.

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANALOG SIGNALS The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement.
TXOUT	AA	**Transmitter Analog Output.** TXOUT can supply a maximum of 2.5 ± 1.015 volts into a minimum load resistance of 10K ohms. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of (57471.26 S)/[(S + 11547.34)(S+57.47)].
RXIN	AB	**Receiver Analog Input.** The RXIN input impedance is >1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of (8474.57 S)/[(S + 11547.34)(S+84.75)]. The maximum input level into the anti-aliasing filter should not be greater than 0 dBm. The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband. Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms.
		EYE DIAGNOSTIC INTERFACE Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX EYEY	OA OA	**Serial Eye Pattern X Output.** **Serial Eye Pattern Y Output.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters. EYEX and EYEY outputs are 10-bit words with their sign bits repeated. The 10-bit data words are shifted out sign bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 576 kHz clock. EYECLK is used to generate a 144 kHz clock (EYECLK*) through an external 74HC74 flip-flop in order to shift EYEX and EYEY data into the serial-to-parallel converters.
EYECLKX	OA	**Shift Serial Eye Pattern Clock (100-Pin PQFP Only).** EYECLKX is a 144 kHz clock derived from EYECLK. It is used to shift EYEX and EYEY data into the serial-to-parallel converters as an alternative to using the the EYECLK output connected to an external 74HC74 flip-flop for EYECLK* generation.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a 9600 Hz strobe used for loading the eye pattern D/A converters.
		GENERAL PURPOSE INPUT/OUTPUT LINES Thirteen general purpose input/output (eight GPIO) and general purpose input (five GPI) pins are available to the user.
GP2- GP7, GP11, GP13	I/O	**General Purpose Input/Output (GPIO).** The direction, input status, and the output data are accessed via DSP RAM read/write. (see Table 13).
GP16- GP17, GP19-GP21	I	**General Purpose Input (GPI).** The input status is accessed via DSP RAM read. (see Table 13).

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty two 8-bit registers, labeled register 00 through 1F (Figure 7). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Table 12 defines the interface memory bits. In Table 12, interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

DSP RAM consists of 16-bit words organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud, or sample time, as selected by the BR1 and BR2 bits. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz except for Group 2 where it is 10368 Hz, and in the voice mode configuration where it is programmable.

The DSP RAM access functions, codes, and registers are identified in Table 13.

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-xx0-xx0
	1E	B2IA	B1IA	B2I1E	B2I2E	B2A	B1I1E	B1I2E	B1A	--00-00-
High Speed Control & Status	1D	SHPR	ASPEED	PR	PRDET	—	—	—	—	00--xxxx
DTMF Status	1C	EDET	DTDET	OTS	DTMFD	DTMF				--------
Not Available	1B	—	—	—	—	—	—	—	—	xxxxxxxx
	1A	—	—	—	—	—	—	—	—	xxxxxxxx
	19	—	—	—	—	—	—	—	—	xxxxxxxx
	18	—	—	—	—	—	—	—	—	xxxxxxxx
	17	—	—	—	—	—	—	—	—	xxxxxxxx
	16	—	—	—	—	—	—	—	—	xxxxxxxx
RAM Access 2 Control & Status and HDLC Control	15	ACC2	AREX2	AEOF	DR2	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status and Group 2 Control	0F	FED		—	—	—	—	CTSP	CDET	--xxxx--
	0E	FSKFLS	—	—	—	—	—	—	—	-xxxxxx
	0D	RX	PNDET	—	—	G2FGC	—	—	—	--xx0xxx
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	xx------
Programmable Interrupts	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC	FSK7E	G2CTK/ DCABLE	—	---0--0x
Mode Control*	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	0	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Programmable Interrupt Control	05	ACC1	AREX1	PIDR	DR1	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES:
* A changed value in these registers (except RTSP and TDIS) require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- This symbol in the "Default Value " column indicates that the value is determined by operating conditions.

Figure 7. R144EFXL DSP Interface Memory Map

Table 12. Modem Interface Memory Bit Definitions

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
12TH	08:4	0	**Select 12th Order.** When control bit 12TH is a 1, the tone detectors operate as one 12th order filter (uses FR3). When 12TH is a 0, the tone detectors operate as three parallel independent 4th order filters (FR1, FR2, FR3). The 12TH bit is valid in FSK, FSK and DTMF receiver, voice, Group 2, or tone receive modes, i.e., CONF = 20h, 21h, 82h, 40h, or 80h, respectively (RTSP and $\overline{RTS}$ off).
ABIDL	09:3	–	**Abort/Idle.** When the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is set) and the modem will send at least eight continuous ones (if ZEROC is 0) or eight continuous zeros (if ZEROC is 1). To stop continuous one or zero transmission, ABIDL must be reset by the host. (HDLC mode only) When the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host. (HDLC mode only)
ACC1	05:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in the AREX1, ADD1 and CR1 bits. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in the AREX2, ADD2, and CR2 bits. WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1, in conjunction with AREX1, contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (02:0-7 and 03:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2, in conjunction with AREX2, contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
AEOF	15:5	0	**Automatic End of Frame.** When the modem is configured as an HDLC transmitter and AEOF control bit is set to a 1, the modem interprets an underrun condition as an end of frame and outputs the FCS and at least one ending flag. (HDLC only.)
ANDOR	0A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled (PIE bit = 1), the modem will assert $\overline{IRQ1}$ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert $\overline{IRQ1}$ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
AREX1	05:6	0	**RAM Access 1 Code Extension Select.** When control bit AREX1 is a 1, the upper part (80h-BFh) of the RAM is selected. When AREX1 is a 0, the lower part (0-7Fh) is selected.
AREX2	15:6	0	**RAM Access 2 Code Extension Select.** When control bit AREX2 is a 1, the upper part (80h-BFh) of the RAM is selected. When AREX2 is a 0, the lower part (0-7Fh) is selected.
ASPEED	1D:6	0	**Auto Speed Change Enable.** When control bit ASPEED is reset to a 0, the modem transmitter sends the default V.17 rate sequence for all V.17 modes. The modem receiver stores the rate sequence in RAM (see Table 13). **ASPEED** / **Data Rate** / **Rate Sequence Pattern** 0 / V.17, all rates / 0111h 1 / 14400 bps / 0171h 1 / 12000 bps / 01B1h 1 / 9600 bps / 01F1h 1 / 7200 bps / 0331h

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
			When set to a 1, the modem transmitter sends a different rate sequence depending on the selected TCM configuration. When receiving in a TCM configuration, the modem reconfigures to the received rate sequence. The new configuration is reflected in the receiver CONF register.
B1A	1E:0	–	**Buffer 1 Available.** When set to a 1, status bit B1A signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (00:0-7). This condition can also cause $\overline{IRQ1}$ or $\overline{IRQ2}$ to be asserted (see B1I1E, B1I2E, and B1IA). The host writing to or reading from register 00 resets the B1A and B1IA bits to 0. (See B1I1E, B1I2E, and B1IA.)
B1I1E	1E:2	0	**Buffer 1 Interrupt 1 Enable.** When control bit B1I1E is a 1, $\overline{IRQ1}$ is enabled for Buffer 1, i.e., the modem will assert $\overline{IRQ1}$ and set B1IA to a 1 when B1A is set to 1 by the modem. When B1I1E is a 0, B1A has no effect on $\overline{IRQ1}$ and B1IA. (See B1A and B1IA.)
B1I2E	1E:1	0	**Buffer 1 Interrupt 2 Enable.** When control bit B1I2E is a 1, $\overline{IRQ2}$ is enabled for Buffer 1, i.e., the modem will assert $\overline{IRQ2}$ when B1A is set to 1 by the modem. When B1I2E is a 0, B1A has no effect on $\overline{IRQ2}$. (See B1A.)
B1IA	1E:6	–	**Buffer 1 Interrupt Active.** When Buffer 1 interrupt is enabled (B1I1E is a 1) and B1A is set to a 1 by the modem, the modem asserts $\overline{IRQ1}$ and sets status bit B1IA to a 1 to indicate that B1A caused the interrupt. The host writing to or reading from register 00 resets B1IA to a 0. (See B1I1E and B1A.)
B2A	1E:3	–	**Buffer 2 Available.** When set to a 1, status bit B2A signifies that, when the modem is in the parallel data mode (with or without HDLC selected), it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of B2A to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). These conditions can also cause $\overline{IRQ1}$ or $\overline{IRQ2}$ to be asserted. The host writing to or reading from register 10h resets the B2A and B2IA bits to 0. (See B2I1E, B2I2E, and B2IA.)
B2I1E	1E:5	0	**Buffer 2 Interrupt 1 Enable.** When control bit B2I1E is a 1, $\overline{IRQ1}$ is enabled for Buffer 2, i.e., the modem will assert $\overline{IRQ1}$ and set B2IA to a 1 when B2A is set to a 1 by the modem. When B2I1E is a 0, B2A has no effect on $\overline{IRQ1}$ and B2IA. (See B2A and B2IA.)
B2I2E	1E:4	0	**Buffer 2 Interrupt 2 Enable.** When control bit B2I2E is a 1, $\overline{IRQ2}$ is enabled for Buffer 2, i.e., the modem will assert $\overline{IRQ2}$ when B2A is set to a 1 by the modem. When B2I2E is a 0, B2A has no effect on $\overline{IRQ2}$. (See B2A.)
B2IA	1E:7	–	**Buffer 2 Interrupt Active.** When Buffer 2 interrupt is enabled (B2I1E is a 1) and B2A is set to a 1 by the modem, the modem asserts $\overline{IRQ1}$ and sets status bit B2IA to a 1 to indicate that B2A caused the interrupt. The host writing to or reading from register 10 resets B2IA to a 0. (See B2I1E and B2A.)
BR1	05:2	1	**Baud Rate 1.** When control bit BR1 is a 1, RAM access for ADD1 occurs at the baud rate regardless of the state of DR1; when BR1 is a 0, RAM access occurs at the sample rate or data rate (See DR1). The BR1 bit must be reset to a 0 for Group 2, tone, or voice mode.
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is a 1, RAM access for ADD2 occurs at the baud rate regardless of the state of DR2; when BR2 is a 0, RAM access occurs at the sample rate or data rate (See DR2). The BR2 bit must be reset to a 0 for Group 2, tone, or voice mode.
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or is in the process of training.

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
CONF	06:0-7	14	**Configuration.** The CONF control bits select the transmitter/receiver configuration: **CONF (Hex) Configuration** 31 V.33/V.17 14400 bps 32 V.33/V.17 12000 bps 34 V.17 9600 bps 38 V.17 7200 bps 71 TCM 14400 bps with 1700 Hz carrier 72 TCM 12000 bps with 1700 Hz carrier 74 TCM 9600 bps with 1700 Hz carrier 78 TCM 7200 bps with 1700 Hz carrier 14 V.29 9600 bps 12 V.29 7200 bps 11 V.29 4800 bps 0A V.27 4800 bps 09 V.27 2400 bps 20 V.21 Channel 2 300 bps (FSK) 21 Transmit: V.21 Channel 2 300 bps (FSK) Receive: V.21 Channel 2 300 bps and DTMF Detector (FSK/DTMF) 40 Group 2 (G2) 80 Transmit: Dual Tone Receive: Tone Detector 82 Transmit: Voice Mode Receive: Tone Detector and Voice Mode **Configuration Definitions:** **V.33.** The modem operates as specified in CCITT Recommendation V.33. **V.17.** The modem operates as specified in CCITT Recommendation V.17. **V.29.** The modem operates as specified in CCITT Recommendation V.29. **V.27.** The modem operates as specified in CCITT Recommendation V.27. **V.21 Channel 2.** The modem operates as specified in CCITT Recommendation V.21 Channel 2 (see Section 3.2.4). **V.21 Channel 2 and DTMF Receiver.** The modem operates as specified in CCITT Recommendation V.21 Channel 2 and detects DTMF transmissions (see Section 3.2.4). **Group 2.** The modem operates as specified in CCITT Recommendation T.3. **Dual Tone Transmit.** The modem transmits single or dual frequency tones in response to the $\overline{\text{RTS}}$ input pin or RTSP bit. Tone frequencies and amplitudes are programmable in DSP RAM. **Tone Detect.** The modem receives a single frequency tone (see FR1, FR2, FR3, and 12TH bits and Section 6). **Voice Mode.** The A/D and the D/A converters are available for voice reception and transmission (see Section 3.2.3). **High Speed Modes.** The 2400 bps through 14400 bps modes.
CR1	05:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, AREX1 and ADD1 address Coefficient RAM. When CR1 is a 0, AREX1 and ADD1 address Data RAM. This bit must be set according to the desired RAM address (Table 4-1).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, AREX2 and ADD2 address Coefficient RAM. When CR2 is a 0, AREX2 and ADD2 address Data RAM. This bit must be set according to the desired RAM address (Table 4-1).
CRC	09:1	–	**Cyclic Redundancy Check Error.** When status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC changes immediately before EOF is set to a 1. (HDLC mode only)
CTSP	0F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD (PDM bit = 0) or DBUFF (PDM bit = 1) will be transmitted. CTSP parallels the operation of the $\overline{\text{CTS}}$ pin.

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
DATA	0C:5	–	**Data Mode.** When status bit DATA is a 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode (PDM bit = 1), the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first.
DCABLE	08:1	0	**Digital Cable Equalizer Enable.** Control bit DCABLE enables (1) or disables (0) insertion of the high speed digital cable equalizer into high speed receive and transmit paths.
DR1	05:4	0	**Data Rate 1.** When control bit DR1 is a 1, RAM access associated with ADD1 occurs at the modem data rate if BR1=0. When DR1 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR1 bit. The DR1 bit is valid only in high speed, FSK/DTMF, or FSK modes.
DR2	15:4	0	**Data Rate 2.** When control bit DR2 is a 1, RAM access associated with ADD2 occurs at the modem data rate if BR2 = 0. When DR2 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR2 bit. The DR2 bit is valid only in high speed, FSK/DTMF, or FSK modes.
DTDET	1C:6	–	**Dual Tone Detected.** When configured as a FSK/DTMF receiver, the modem sets status bit DTDET to a 1 when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMF Output Word (1C:0-3) value is available when DTDET is set. If the received signal is a valid DTMF signal, then DTDET will be set to a 1 approximately 11 ms following EDET setting to a 1. The DTDET bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
DTMF	1C:0-3	–	**DTMF Output Word.** When the modem is configured as a FSK/DTMF receiver and a DTMF tone is present such that status bit DTDET is set to a 1 by the modem, the encoded DTMF output is written into 1C:0-3. The DTMF symbol codes are: **DTMF Symbol / Encoded Output (Hex) / DTMF Symbol / Encoded Output (Hex)** 1 0 3 8 4 1 6 9 7 2 9 A * 3 # B 2 4 A C 5 5 B D 8 6 C E 0 7 D F
DTMFD	1C:4	–	**DTMF Signal Detected.** When configured as a FSK/DTMF receiver, the modem sets status bit DTMFD to a 1 when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading the DTMF Output Word (1C:0-7), otherwise two or more detections of the same symbol may be missed by the host.
EDET	1C:7	–	**DTMF Early Detection.** When configured as a FSK/DTMF receiver, the modem sets status bit EDET to a 1 approximately 20 ms after the DTMF signal energy is detected to indicate that the received signal is probably a DTMF signal. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
EOF	09:2	–	**End of Frame.** When the modem is configured as a transmitter and bit AEOF is 0, the EOF bit is a control bit. When AEOF is a 0, to convey to the modem that it is time to send the 16-bit FCS and ending flag of a HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (B2A sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a transmitter and bit AEOF is a 1, EOF is a status bit. In this case, the modem will interpret the underrun condition as the end of the frame, set EOF, and will output the 16-bit FCS and at least one ending flag. EOF is reset whenever a flag is transmitted. (HDLC mode only). When the modem is configured as a receiver and status bit EOF is a 1, the modem has received a frame ending flag and bit CRC is updated. EOF must be reset by the host before receiving the ending flag of a following frame. (HDLC mode only).

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training. (See status bit P1.)
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. For short train only, this bit is used in conjunction with the SHTR bit.
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicate the level of the received signal according to the following codes: **FED (Hex) — Energy Level** 0 — No energy (idle mode) 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold
FLAG	09:0	–	**FLAG Mode.** When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode only)
FR1	08:5	–	**Frequency No. 1.** The modem sets status bit FR1 to a 1 when energy above tone detector 1's turn-on threshold is detected. The default detection range = 2100 Hz ± 25 Hz. FR1 is valid in FSK, FSK and DTMF receiver, voice, Group 2, or tone receive modes, i.e., CONF = 20h, 21h, 40h, 82h, or 80h, respectively (RTSP and $\overline{\text{RTS}}$ off).
FR2	08:6	–	**Frequency No. 2.** The modem sets status bit FR2 to a 1 when energy above tone detector 2's turn-on threshold is detected. The default detection range = 1100 Hz ± 30 Hz. FR2 is valid in FSK, FSK and DTMF receiver, voice, Group 2, or tone receive modes, i.e., CONF = 20h, 21h, 40h, 82h, or 80h, respectively (RTSP and $\overline{\text{RTS}}$ off). (See Section 6.)
FR3	08:7	–	**Frequency No. 3.** The modem sets status bit FR3 to a 1 when energy above tone detector 3's turn-on threshold is detected, The default detection range = 462 Hz ±14 Hz. FR3 is valid in all receive modes (RTSP and $\overline{\text{RTS}}$ off). (See Section 6.)
FSK7E	08:2	–	**FSK FLAG (7E) Detected.** The modem sets status bit FSK7E to a 1 when FSK flags have been detected in a high speed receiver mode. FSK7E is valid after bit FSKFLS transitions from 1 to 0. FSK7E is not valid in V.27 ter short train mode.
FSKFLS	0E:7	0	**FSK FLAG (7E) Search.** When status bit FSKFLS is a 1, the modem is searching for FSK flags in high speed receiver modes except V.27 ter short train. This bit is reset to 0 by the modem when the FSK flag search is completed.
G2CTK	08:1	0	**Group 2 External Clock Tracking Enable.** Control bit G2CTK selects tracking of either the internally generated clock (G2CTK = 0) or the external clock input on the G2XCLK pin (G2CTK = 1). (Group 2 only.)
G2FGC	0D:3	0	**Group 2 Fast Gain Control.** When control bit G2FGC is a 1, fast AGC rate (8.6 times the standard rate) is selected. G2FGC is valid only in the Group 2 mode.
HDLC	07:0	0	**HDLC Mode.** When control bit HDLC is a 1 and the PDM bit is a 1, the modem performs HDLC framing in parallel data mode. When the HDLC bit is a 0 or the PDM bit is a 0, the modem does not perform HDLC framing. (See the SETUP bit.)
IO1	05:3	0	**Input/Output RAM 1 Select.** When control bit IO1 is set, ADD1 addresses IO RAM. When IO1 is reset, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 13.)

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
IO2	15:3	0	**Input/Output RAM 2 Select.** When control bit IO2 is set, ADD2 addresses IO RAM. When IO2 is reset, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 13.)
ITADRS	0A:0-4	0	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take effect. The address of the byte on which the modem asserts IRQ1 on a bit or bits in that byte is:
ITBMSK	0B:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQ1 on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OTS	1C:5	–	**DTMF On-Time Satisfied.** When configured as a FSK/DTMF receiver, the modem sets status bit OTS to 1 after the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy the DTMF off-time criteria. (See Section 4.2.)
OVRUN	09:7	–	**Overrun/Underrun.** When configured as a transmitter and control bit AEOF is a 0, the modem sets status bit OVRUN to a 1 if a transmit underrun condition occurs. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL bits will be set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host re-sets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if B2A is reset) or will transmit continuous flags. The modem will reset OVRUN every time it sets B2A. If AEOF is a 1, OVRUN is disabled. When the configured as a receiver, the modem sets the OVRUN bit to a 1 if a receive over-run condition occurs. To detect the next overrun condition, the host must reset this bit.The OVRUN bit is valid only in HDLC mode.
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being sent. The P1 sequence is an echo protection tone. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being sent. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.

Host Register (Hex)	ITADRS (Hex)	Host Register (Hex)	ITADRS (Hex)
00	00	10	08
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
PDM	07:5	0	**Parallel Data Mode.** When control bit PDM is a 1, parallel data mode is selected. If the modem is a transmitter, data for transmission is accepted from DBUFF (10:0-7). If the modem is a receiver, the modem provides received data to DBUFF (10:0-7) and to the RXD output pin. When the PDM bit is a 0, serial data mode is selected. If the modem is a transmitter, data for transmission is accepted from the TXD input pin. When the modem is a receiver, the modem provides the received data only to the RXD output pin. (See HDLC bit.)
PIA	1F:7	–	**Programmable Interrupt Active.** When the programmable interrupt is enabled (control bit PIE is a 1) and if control bit PIREQ has been previously reset by the host, the modem asserts IRQ1 and sets status bit PIA to a 1 to indicate that PIREQ caused the interrupt request. The PIA bit is reset when the host resets either the PIREQ bit or the PIE bit to a 0. (See PIE and PIREQ.)
PIDR	05:5	0	**Programmable Interrupt at Data Rate.** When control bit PIDR is a 1, the programmable interrupt runs at the data rate. When PIDR is a 0, the programmable interrupt runs at the sample rate (9600 Hz). The PIDR bit is valid in all modes except Group 2, tone, and voice.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is a 1, modem will assert IRQ1 and set PIA to a 1 when PIREQ is set to a 1 by the modem. When PIE is a 0, PIREQ has no effect on IRQ1 and PIA. (See PIA and PIREQ.)
PIREQ	1F:3	–	**Programmable Interrupt Request.** When set to a 1, status bit PIREQ indicates that the interrupt condition specified by ITBMSK, ITADRS, TRIG, and ANDOR is true. The host must reset the PIREQ bit after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ1. (See PIA and PIE.)
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 indicates the PN sequence is being sent. When PN = 0, the PN sequence is not being sent. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN sequence is being received. When PN = 0, the PN sequence is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is a 1, the receiver has detected the PN portion of the training sequence. When PNDET is a 0, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is a 1, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is a 0, a successful training has not occurred. PNSUC is still valid after the CDET bit is set to a 1.
PR	1D:5	–	**Rate Sequence Period.** When status bit PR is set to a 1 during transmit, the modem is sending the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being sent. When set to a 1 during receive, the modem is receiving the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being received. The PR bit is valid only in V.33 or V.17 modes. (See Figure 3-4.)
PRDET	1D:4	–	**Rate Sequence Detection.** When status bit PRDET is set to a 1, the modem receiver has detected a rate sequence pattern containing a proper synchronization bit pattern. The PRDET bit is valid only in V.33 or V.17 modes.
RTSP	07:7	0	**Request To Send Parallel.** The one state of control bit RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset to a 0 (or RTS is turned off) and the turn-off sequence has been completed. RTSP parallels the operation of the RTS hardware input pin. These inputs are "ORed" by the modem.
RX	0D:7	–	**Receive State.** When status bit RX is a 1, the modem is in the receive state; when RX is a 0, the modem is in the transmit state. (See RTSP.)

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1= 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being sent. When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP must be set to a 1 by the host after the host writes a configuration code into the CONF bits (06:0-7) or changes any of bits 0 through 5 in register 07h (07:0-5). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change is implemented.
SHPR	1D:7	0	**Short Train Rate Sequence.** When control bit SHPR is set to a 1, the V.33/V.17 rate sequence is included in the short training sequence, which extends the training by 64 bauds.
SHTR	07:4	0	**Short Train Mode.** When control bit SHTR is a 1 and CONF is 31h, 32h, 34h, 38h, 71h, 72h, 74h, 78h, 14h, 12h, 11h, 0Ah, or 09h, the modem will perform a short training sequence. A successful long train at the same data rate must precede its short train. A successful V.17 long train at any data rate must precede its short train. The setting of the SHTR bit, along with the setting of the EQSV and EQFZ bits, must be followed by the setting of the SETUP bit.
SIDLE	0C:0	–	**Silence/Idle.** When the modem is configured as a high speed transmitter, status bit SIDLE = 1 indicates the modem is transmitting silence. When the modem is configured as a high speed receiver, SIDLE = 1 indicates the modem is waiting for energy or idling.
SQEXT	07:2	0	**Squelch Extend.** Control bit SQEXT determines the length of time the modem receiver is inhibited from receiving any signal after transmitter turn-off. The length of time is either 20 ms (SQEXT = 0) or 140 ms (SQEXT = 1).
TDIS	07:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when the RTS pin or RTSP bit is activated.
TRIG	0A:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE bit = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC level triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **TRIG (Hex) — Description** 0 — DC Level Triggered 1 — Positive Edge Triggered 2 — Negative Edge Triggered 3 — Edge Triggered
WRT1	05:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is set to a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by AREX1, ADD1, and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by AREX1, ADD1, and CR1, and stores the data into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is a 1 and ACC2 is set to a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by AREX2, ADD2, and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is set to a 1, the modem reads data from its internal RAM from the locations addressed by AREX2, ADD2, and CR2, and stores the data into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Loc. (Hex)	Default Value (Hex)	Name/Description
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** When control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is 0, ZEROC is disabled. The ZEROC bit is valid only in HDLC mode.

Table 13. Modem DSP RAM Access Codes

No.	Function	DRx	BRx	CRx	IOx	AREXx	ADDx (Hex.)	Read Reg. No.
1	Received Signal Sample	0	0	0	0	0	15	2,3
2	Received Signal Sample (Voice Mode)	0	0	0	0	0	A0	0
3	Average Power	0	0	0	0	0	14	2,3
4	AGC Gain Word	0	0	1	0	0	15	2,3
5	AGC Slew Rate	0	0	0	0	0	95	0,1
6	Tone 1 Frequency	0	0	1	0	0	21	2,3
7	Tone 1 Transmit Output Level	0	0	0	0	0	22	2,3
8	Tone 2 Frequency	0	0	1	0	0	22	2,3
9	Tone 2 Transmit Output Level	0	0	0	0	0	23	2,3
10	Transmit Output Level	0	0	0	0	0	21	2,3
11	Equalizer Tap Coefficients	0	1	1	0	0	3A - 69	0,1, 2,3
12	Rotated Equalizer Output (Eye Pattern)	0	1	1	0	0	17	0,1, 2,3
13	Decision Points (Ideal)	0	1	0	0	0	17	0,1, 2,3
14	Error Vector	0	1	1	0	0	1D	0,1, 2,3
15	Rotation Angle	0	1	1	0	0	0C	0,1
16	Frequency Correction	0	1	1	0	0	18	2,3
17	Eye Quality Monitor (EQM) Hard Decision	0	1	1	0	0	0D	2,3
18	Eye Quality Monitor (EQM) TCM Min. Metric	0	0	1	0	1	00	2,3
19	RLSD Turn-on Threshold	0	0	1	0	0	37	2,3
20	RLSD Turn-off Threshold	0	0	1	0	0	B7	0,1
21	Receiver Sensitivity (MAXG)	0	0	1	0	0	24	2,3
22	Group 2 PLL Frequency Correction	0	0	0	0	0	0D	2,3
23	Group 2 PLL Slew Rate	0	0	0	0	0	18	2,3
24	Group 2 Zero Crossing Threshold (Negative)	0	0	0	0	0	19	2,3
25	Group 2 Zero Crossing Threshold (Positive)	0	0	0	0	0	99	0,1
26	Group 2 AGC Slew Rate	0	0	1	0	0	05	2,3
27	Group 2 Black/White Threshold	0	0	0	0	0	24	2,3
28	Group 2 Phase Limit	0	0	0	0	0	1A	2,3
29	Minimum On Time (DTMF)	0	0	1	0	0	1F	2,3
30	Minimum Off Time (DTMF)	0	0	0	0	0	1F	2,3
31	Minimum Cycle Time (DTMF)	0	0	0	0	0	9F	0,1
32	Maximum Dropout Time (DTMF)	0	0	1	0	0	9F	0,1
33	Maximum Speech Energy (DTMF)	0	0	1	0	0	1E	2,3
34	Frequency Deviation, Low Group (DTMF)	0	0	0	0	0	1D	2,3
35	Frequency Deviation, High Group (DTMF)	0	0	1	0	0	1D	2,3
36	Negative Twist (DTMF)	0	0	0	0	0	1E	2,3
37	Positive Twist (DTMF)	0	0	0	0	0	9E	0,1
38	Maximum Energy Hit Time (DTMF)	0	0	1	0	0	A3	0,1
39	Number of Additional Flags (HDLC)	0	0	1	0	0	85	0,1
40	Transmitter Rate Sequence Pattern	0	0	0	0	0	6B	2,3
41	Receiver Rate Sequence Pattern	0	0	1	0	0	1A	0,1
42	FR1 Tone Detector Coefficients	0	0	1	0	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	0	1	0	0	A5-AA	0,1
43	FR2 Tone Detector Coefficients	0	0	1	0	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	0	1	0	0	AB-B0	0,1
44	FR3 Tone Detector Coefficients	0	0	1	0	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	0	1	0	0	B1-B6	0,1
45	Sample Rate Counter 1, Most Signif. Bit	0	0	0	1	0	2B	0,1
46	Sample Rate Counter 2, Least Signif. Word	0	0	0	1	0	28	0,1
47	Tone Detector Threshold Comparator	0	0	0	0	0	9D	0,1

Table 13. Modem DSP RAM Access Codes (Cont'd)

No.	Function	DRx	BRx	CRx	IOx	AREXx	ADDx (Hex.)	Read Reg. No.
48	GPIO Direction Register, Low Byte (GPDRL)[1]	0	0	0	1	0	33	0,1
49	GPIO Status Register, High Byte (GPSRH)[2]	0	0	0	1	0	37	0,1
50	GPIO Status Register, Low Byte (GPSRL)[2]	0	0	0	1	0	33	0,1
51	GPIO Output Register Low Byte (GPORL)[3]	0	0	0	1	0	B2	0,1
52	12 dB Switchable Gain Disable Bit	0	0	0	1	0	2F	0,1
53	Sleep Mode Enable Bit	0	0	0	1	0	3E	0,1

Notes:

1. Write operation sets the direction of the GPIO pins.
2. Read operation sets the level of the GPIO pins.
3. Write only.

MODEM INTERFACE CIRCUIT

CIRCUIT AND COMPONENTS

The modem is supplied as a 100-pin PQFP or 64-pin QUIP device to be designed into OEM circuit boards. The recommended modem interface circuits (Figures 8 and 9, respectively) illustrate the connections and components required to connect the modem to the OEM electronics.

Resistors R5 and R8 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

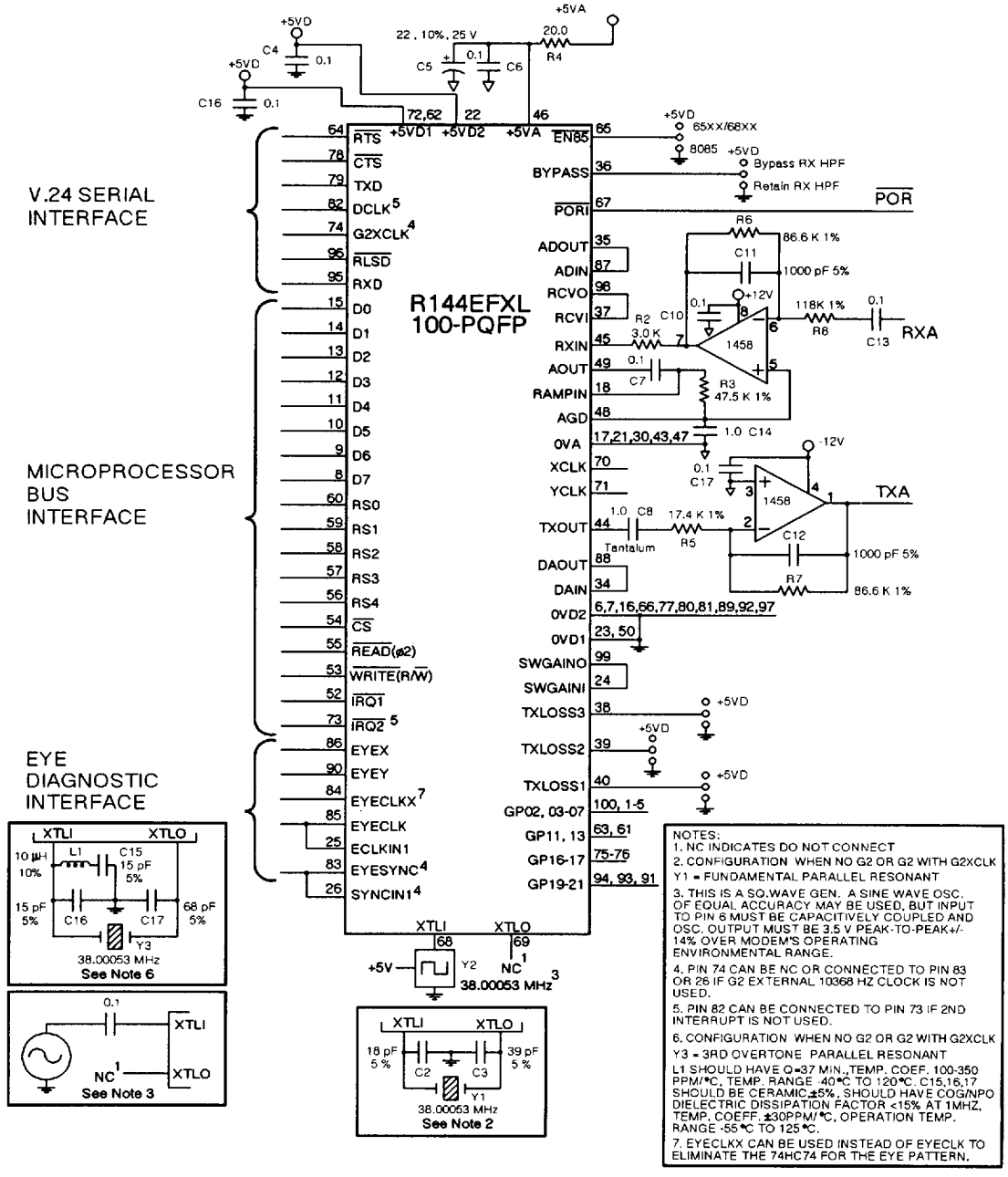

Figure 8. Recommended Modem PQFP Interface Circuit

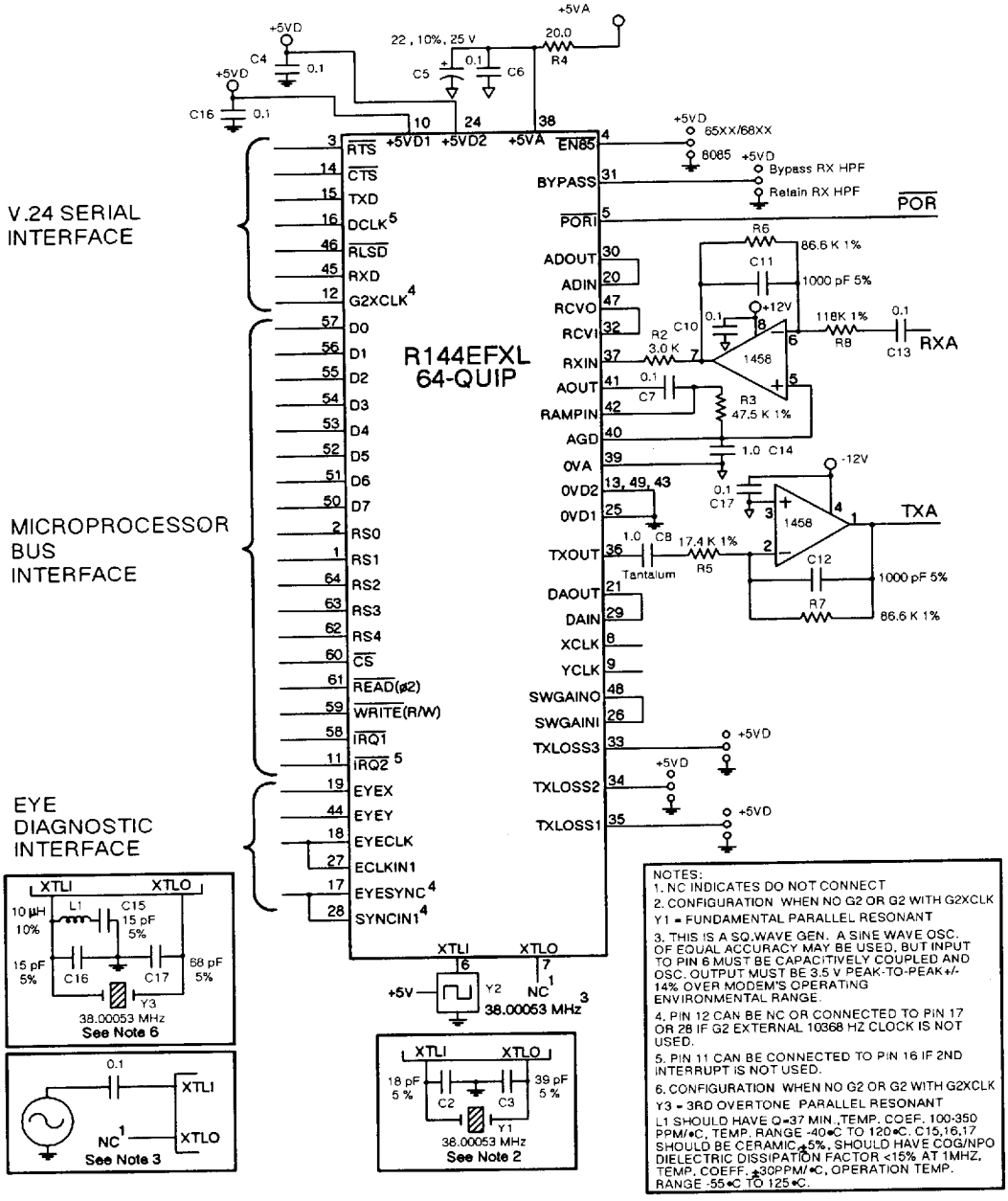

Figure 9. Recommended Modem QUIP Interface Circuit