

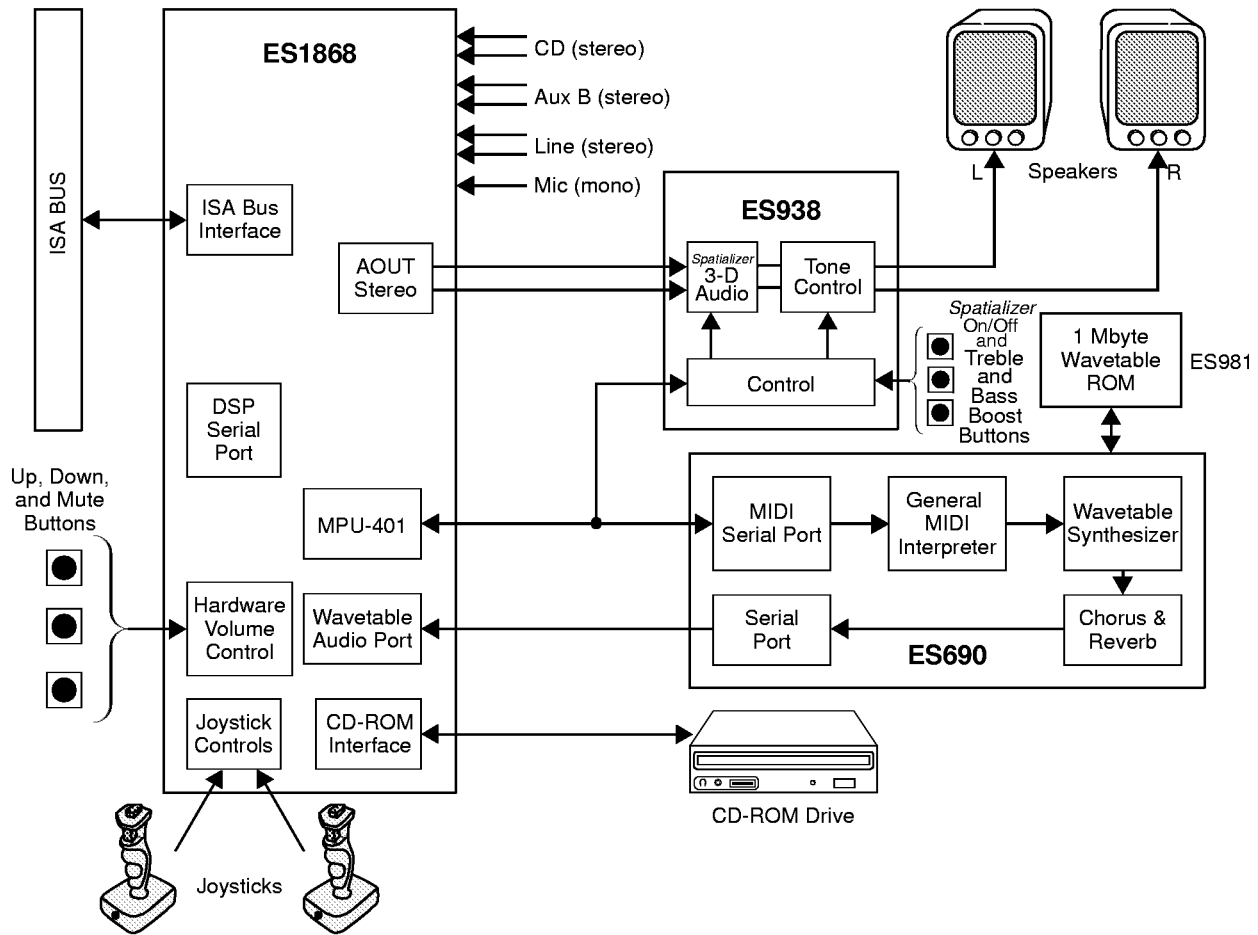


Figure 2 ES1868, ES690, and ES938 PC-based Reference Design Block Diagram

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PINOUT

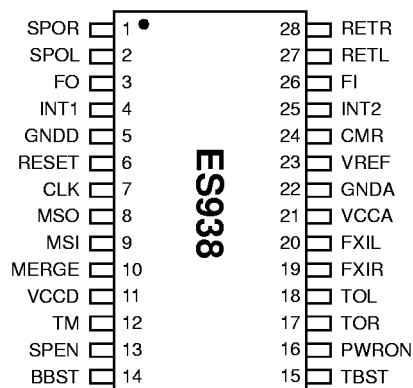


Figure 3 The ES938 Pinout

PIN DESCRIPTIONS

Digital Pin Descriptions

Pin	I/O	Description
VCCD	I	Digital power supply, 3.0 - 5.5 V.
GNDD	I	Digital ground.
CLK	I	14.318 MHz clock input.
RESET	I	Active-high reset input from ISA bus.
TM	I	Test pin; connect to digital ground.
MSO	O	MIDI serial output; connect to MIDI serial input of audio controller.
MSI	I	MIDI serial input; connect to MIDI serial output of audio controller.
MERGE	I	MIDI serial input from external MIDI devices. Except when the ES938 is transmitting, this pin is internally connected to the MSO pin.
SPEN	I	Input with internal pull-down device. When high (digital or analog VCC), enables spatialization effect at current limit level (limit level is set to maximum by reset). The internal pull-down device is disabled when the ES938 is powered down.
TBST	I	Input with internal pull-down device. When high (digital or analog VCC), enables treble boost, overriding current internal tone control setting. The internal pull-down device is disabled when the ES938 is powered down.
BBST	I	Input with internal pull-down device. When high (digital or analog VCC), enables bass boost, overriding current internal tone control setting. The internal pull-down device is disabled when the ES938 is powered down.
PWRON	I	Input with internal pull-down device. When low, the ES938 is powered down.

Analog Pin Descriptions

Pin	I/O	Description
VCCA	I	Analog power supply, 5 V $\pm$ 10%. Should be greater than or equal to VDDD-0.3 V.
GNDA	I	Analog ground.
VREF	O	2.25 V reference resistor divider output. Should be bypassed to analog ground with 0.1 μ F capacitor.
CMR	O	Buffered common mode reference output. Should be bypassed to analog ground with a 47 μ F electrolytic capacitor with a .1 μ F capacitor in parallel.
FXIL	I	Signal input, left channel.
FXIR	I	Signal input, right channel.
SPOL	O	Left channel <i>Spatializer</i> output.
SPOR	O	Right channel <i>Spatializer</i> output.
RETL	I	Left channel tone control input.
RETR	I	Right channel tone control input.
INT1	I	Connect to external 4.7 μ F capacitor (which connects to analog ground).
INT2	I	Connect to external 4.7 μ F capacitor (which connects to analog ground).
FO	O	Output connected to FI via external capacitor/resistor network.
FI	I	Input connected to FO via external capacitor/resistor network.
TOL	O	Left channel output of tone control.
TOR	O	Right channel output of tone control.

FUNCTIONAL DESCRIPTION

MIDI Register Control Interface

The ES938 is controlled from the host processor by using the System Exclusive (Sysex) command through a MIDI serial link. The command format is:

```
F0 <id> <command> <address> <data>  
[<address> <data> ...] F7
```

where:

F0 MIDI System Exclusive start.
<id> Three-byte manufacturer code for ESS Technology. The ID is 00 00 7B
<command> Command for register read is 7E. Command for register write is 7F.
<address> ES938 register address, 00–07H.
<data> Data to be written into register for write command. Not used for read command.
F7 MIDI System Exclusive end.

The register read command responds with a System Exclusive message as follows:

```
F0 <id> 7E <address> F7
```

Register Write System Exclusive Messages

If the host software is not currently doing MIDI I/O, it can simply enable the MPU-401 port and transmit the System Exclusive command to write one or more of the ES938 registers.

If the host software is actively transmitting MIDI data, then the System Exclusive message must be inserted into the data stream in such a way as to not cause a conflict. This means that the host software must keep track of the data being transmitted, so that it can know when it can transmit the System Exclusive message.

1. Do not transmit in the middle of a multi-byte MIDI message. Only transmit between MIDI messages. For example, a note-on message has three bytes (two bytes if it is a Running Status message); do not transmit in the middle of this message. Also, do not transmit in the middle of a System Exclusive message.
2. Keep track of the current Running Status state. After the System Exclusive is transmitted, the Running Status state is probably corrupted by devices receiving the System Exclusive. Therefore, if the next data to be transmitted does not start with a new status byte, insert a status byte. A status byte is defined as a MIDI byte between 80h and F7h.
3. At the time the System Exclusive is transmitted, the Running Status state may be unknown. Or you don't want to send the System Exclusive for reasons listed

above, but a time-out elapses. In either case, after the System Exclusive, discard transmitted bytes up until the next status byte.

Register Read System Exclusive Messages and the MERGE Pin

Normally, the MERGE input is connected to MSO (MIDI Serial Output pin) inside the ES938. When the ES938 is transmitting in reply to a register read command, it must disconnect MERGE and drive MSO.

The ES938 has logic that prevents the switch away from MERGE until 10 bit periods have passed while the MERGE pin remains high. The purpose is to prevent switching while serial data is being transmitted. For this reason, the host software must read and process (or discard) incoming data until the System Exclusive and manufacturer ID bytes are received.

Of course, it is possible that incoming MIDI data to the MERGE pin will be lost while the System Exclusive message is being transmitted. If the host software was in the middle of reading a multi-byte MIDI message, that message must be assumed to be corrupted, and therefore it should be discarded.

At the end of the System Exclusive transmission, the ES938 will switch the MSO pin back to the MERGE pin. However, before it does so, it must see 10 bit periods pass while the MERGE pin remains high.

After the host software receives the System Exclusive message, it should discard Running Status messages until a new status byte is received.

REGISTERS

Register 0 Miscellaneous Control Register

7	6	5	4	3	2	1	0
0	1	TIL	NG	DB			

Reset: 49h

Bit 6 1

Bit 5:4 TIL

Tone Block Input Level. Controls the attenuator at the input of the tone control circuit.

0 0	0 dB
0 1	-3 dB
1 0	-6 dB
1 1	-9 dB

Bit 3:2 NG

Noise Gate.

The setting on these two bits must be:

NG0=0, NG1=1

Bit 1:0 DB

These values must be set to a value of 1 (DB1=0, DB0=1).

Register 1 Tone Control Register

7	6	5	4	3	2	1	0
0	Treble Control	0	Bass Control				

Reset: 33h

Bit 6:4 Treble Control

000	-9 dB
001	-6 dB
010	-3 dB
011	0 dB
100	+3 dB
101	+6 dB
110	+9 dB
111	+12 dB

Bit 2:0 Bass Control

000	-9 dB
001	-6 dB
010	-3 dB
011	0 dB
100	+3 dB
101	+6 dB
110	+9 dB
111	+12 dB

Registers 2, 3, 4 Reserved (Write 0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Register 5 Spatializer Effect Limit/Mode

7	6	5	4	3	2	1	0
0	SPC5	SPC4	SPC3	SPC2	SPC1	SPC0	R

Bit 7:0 Spatializer Mode & Space Control Settings

These bits determine the amount of 3-D effect. Register settings must be:

00h: no effect

47h: minimum effect level

5Bh: medium effect level

67h: maximum effect level

Register 6

Spatializer Processor Enable Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	Spatializer Enable	

Reset: 00H

Bit 1:0 Spatializer Processor Enable Register

02h Disable Spatializer Processor

03h Enable Spatializer Processor

Register 7**Power Control Register**

7	6	5	4	3	2	1	0
R	R	R	R	R	Enable Pullups FXIL/R	Output Enable	Power Down

Reset: 0Eh**Bit 7:3** **Reserved****Bit 2** **Enable Pullups FXIL, FXIR**

- 0: No pullups to 2.25 V on pins FXIL, FXIR when powered down.
- 1: Pullups enabled when powered down (except when input PWRON=0, in which case the pullups are always defeated).

Bit 1: **Output Enable**

0: Output Bypass

1: Output Enable

When bit 1 is 0, the entire ES938 analog section is bypassed. Outputs TOL and TOR are internally connected to inputs FXIL and FXIR. Inputs FXIL and FXIR have high-value pullups to approximately the voltage of the CMR. Bypass is also enabled when powered down when the reset input is high.

Bit 0 **Power Down**

0: Power Up

1: Power Down

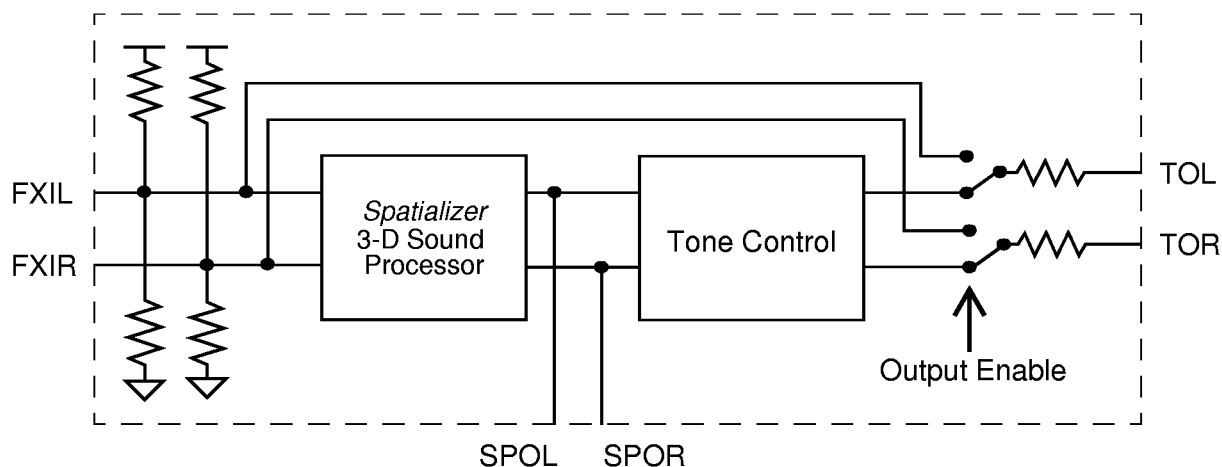
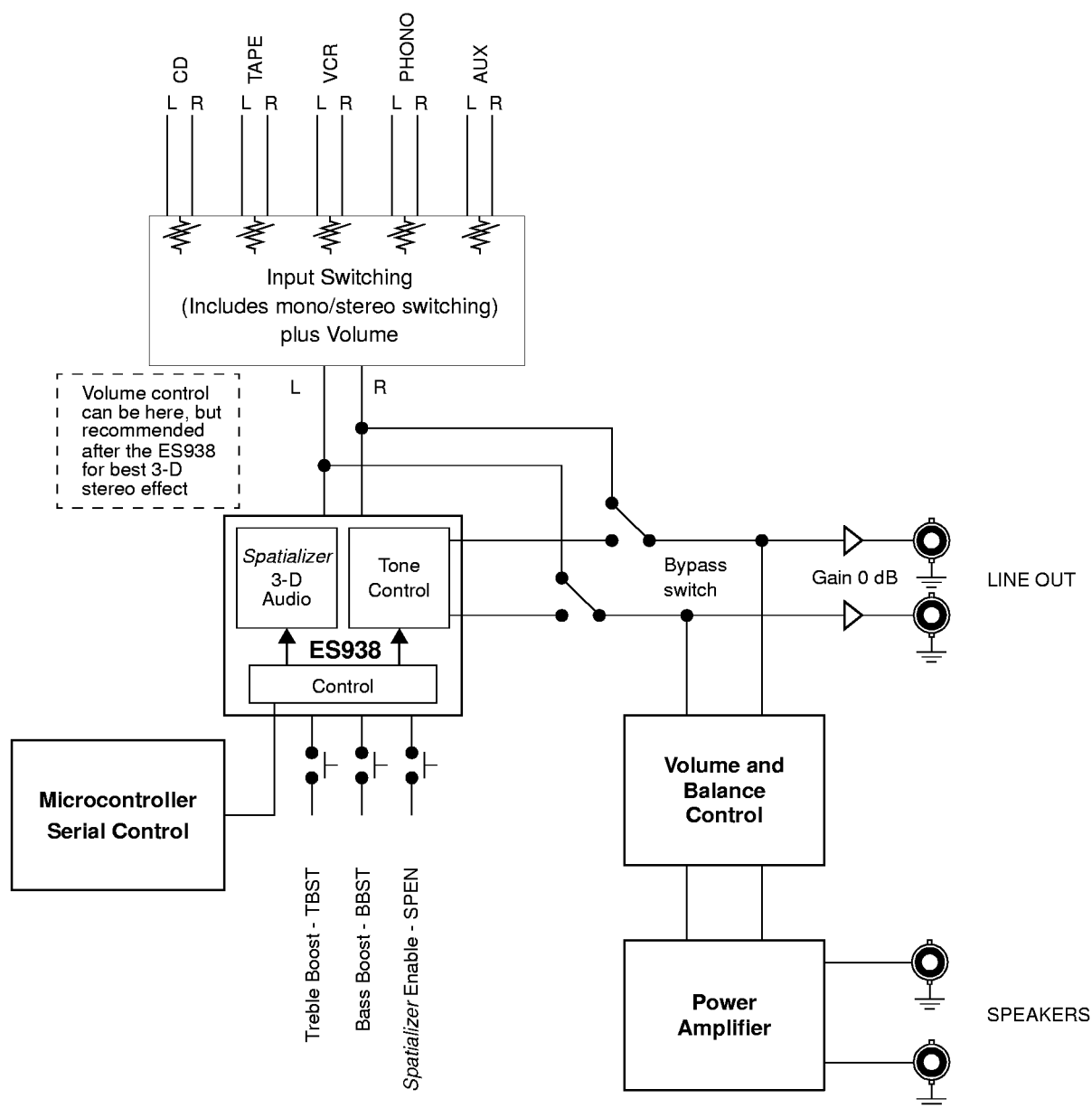


Figure 4 Output Bypass During Power Down and Reset

TYPICAL CONSUMER AUDIO ELECTRONICS APPLICATION

 Figure 5 Typical *Spatializer* Implementation

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Rating	Symbol	Value
Analog supply voltage	VDDA	-0.3 to 7.0 V
Digital supply voltage	VDDD	-0.3 to 7.0 V
Input voltage	VIN	-0.3 to 7.0 V
Operating temperature range	TA	0 to 70 °C
Storage temperature range	TSTG	-50 to 125 °C

DC Electrical Characteristics

(over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Comments
VIH	High-level input voltage	2.0	VCC +0.25	V	All inputs TTL level except CLK
VIL	Low-level input voltage	-0.3	0.8	V	All inputs TTL level except CLK
VCH	CLK high-level input	2.0	VCC +0.25	V	TTL level input
VCL	CLK low-level input	-0.3	0.8	V	TTL level input
VOH	High-level output voltage	3.0	–	V	IOH = 1mA
VOL	Low-level output voltage	–	0.45	V	IOL = 4mA
ILI	Input leakage current	–	±15	μA	
ILO	Output leakage current	–	±15	μA	
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CO	Input/output capacitance	–	12	pF	fc = 1 MHz
CCLK	CLK capacitance	–	20	pF	fc = 1 MHz

Extended DC Electrical Characteristics

(over recommended operating conditions)

Parameter	Pins (Conditions)	Min	Typ	Max	Unit
Reference voltage	VREF, CMR	2.00	2.25	2.50	V
Input impedance	FXIL, FXIR	75k	100k	125k	Ω
Output impedance	SPOL, SPOR	750	1k	1.25k	Ω
	TOL, TOR	5k	7.5k	10k	Ω
Max voltage output swing	TOL, TOR	-	2.5	-	Vpp
IDDD operating current	(CLK running)	-	500	1k	μA
	(CLK stopped)	-	10	50	μA
IDDA operating current	(Power up)	-	10	20	mA
	(Power down)	-	10	50	μA

AC Electrical Characteristics

(over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	Total clock cycle time	-	$14.31818 \pm 0.5\%$	-	MHz
t_H	Clock cycle high	40	70	100	ns
t_L	Clock cycle low	40	70	100	ns
t_{bit}	MIDI bit period	-	$32.0 \pm 0.5\%$	-	μs

Timing Diagrams

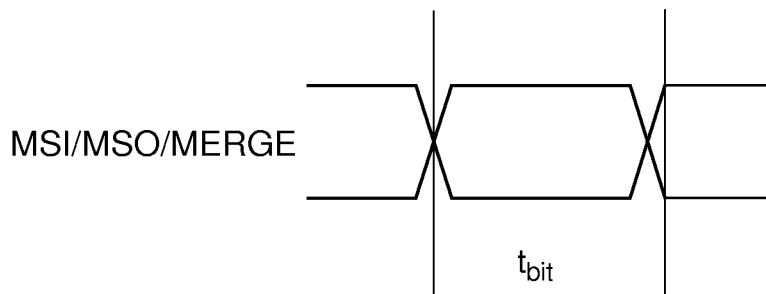
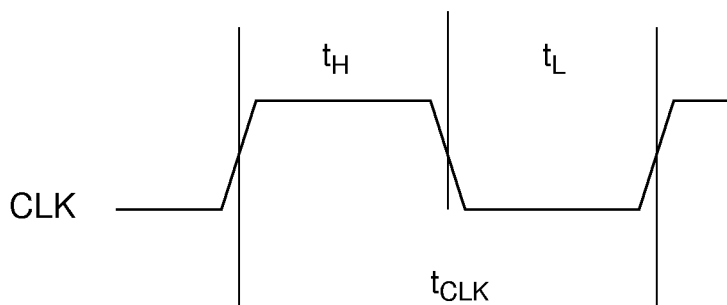
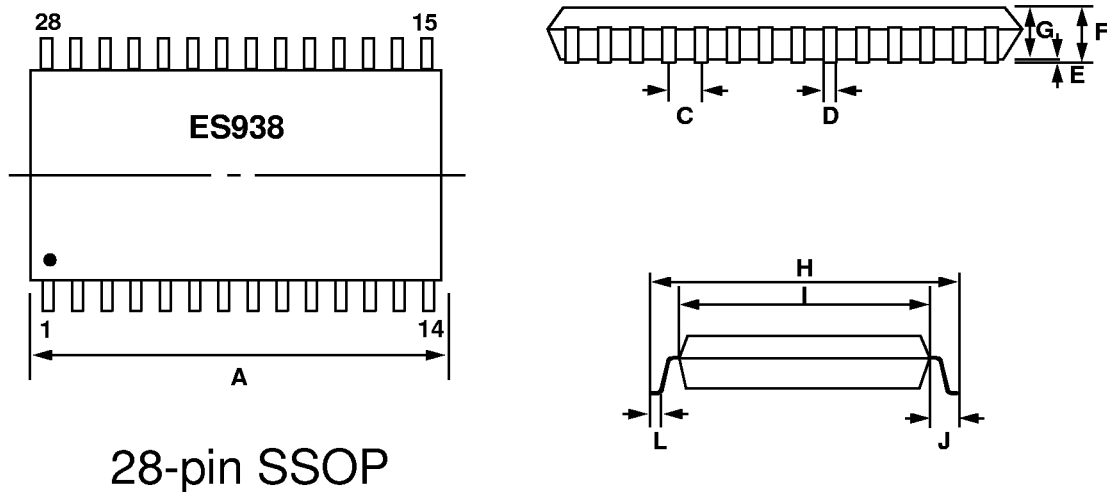


Figure 6 Clock Timing Diagrams

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
A	Package's Outside, X-axis	10.07	10.20	10.33
C	Lead pitch	-	0.65	-
D	Lead width	0.25	-	0.38
E	Board standoff	0.05	0.13	0.21
F	Package height	1.73	1.86	1.99
G	Package thickness	1.68	1.73	1.78
H	Foot print	7.65	7.80	7.90
I	Package's width, Y-axis	5.20	5.30	5.38
J	Lead length	-	1.25	-
L	Foot length	0.63	0.75	0.95
-	Coplanarity	-	-	0.076
-	Leads in x-axis	-	14	-
-	Total Leads	-	28	-
-	Package Type	-	SSOP	-

Figure 7 Mechanical Dimensions

APPENDIX A: ES938 SCHEMATIC

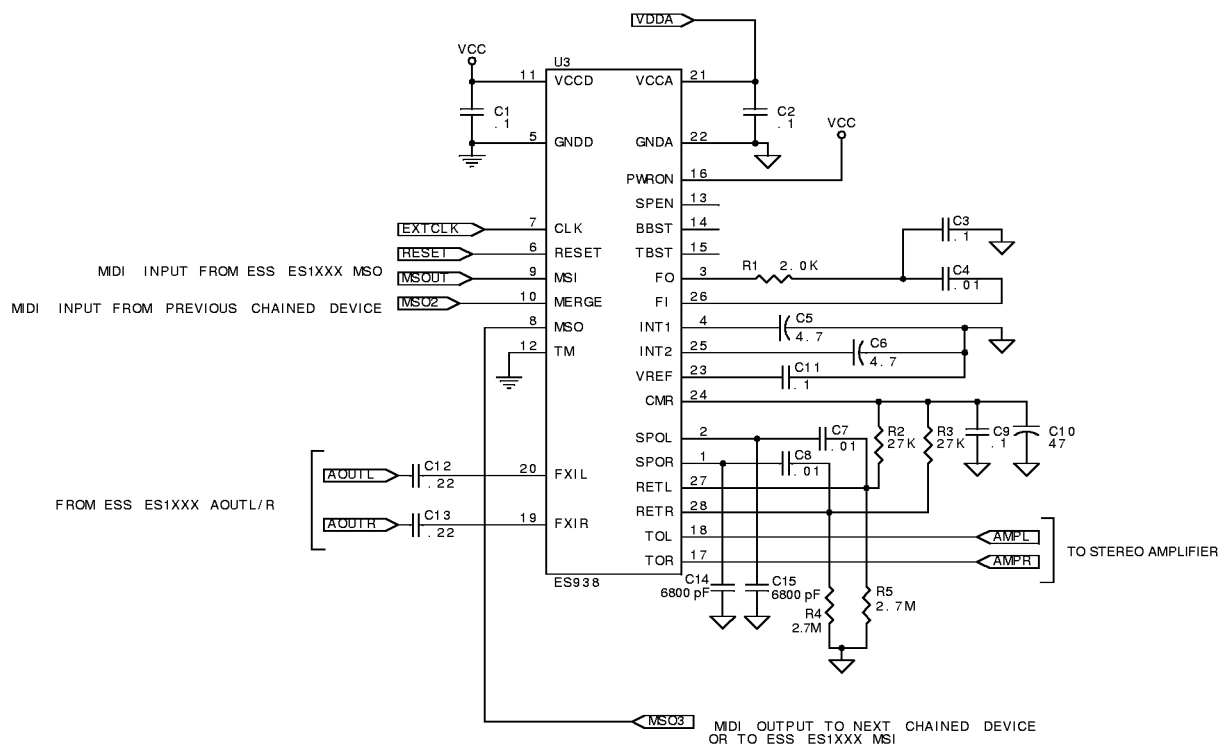


Figure 8 ES938 Schematic

APPENDIX B: ES938 SCHEMATIC BILL OF MATERIALS (BOM)

Item	Quantity	Reference	Part
1	5	C1, C2, C3, C9, C11	0.1 μ F
2	2	C12, C13	0.22 μ F
3	3	C4, C7, C8	0.01 μ F
4	1	C10	47 μ F
5	2	C5, C6	4.7 μ F
6	2	C14, C15	6800 pF
7	1	R1	2k
8	2	R2, R3	27k
9	2	R4, R5	2.7M
10	1	U3	ES938 SSOP



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