Integrated Device Technology, Inc.

LASER PRINTER Integrated System Controller for IDT R30xx RISController™ Family with Adobe Frame Buffer Compression

IDT79R3740 ADVANCE DATA

FEATURES:

- Integrated system controller for low cost, high resolution, high performance, laser printer controllers
  - Direct interface to IDT R3041™, R3051™, R3052™, R3071™ and R3081™ pin-compatible RISControllers™
  - Supports bus interface frequencies from 16 to 33MHz
- Incorporates Adobe Frame Buffer Compression
  - Achieves greater than 4:1 lossless compression for most pages of reasonable complexity, lowering DRAM cost up to 4MB for 600 dpi, 8½" x 11" printers
  - Supports range of printer strategies, from "print all pages" with minimum memory cost (by switching to 300 dpi for page complexities that require more DRAM), to requiring more memory to print fully compressed, high quality pages at maximum perfomance
  - Supports printer page rates up to 20 ppm
- On-chip DRAM controller for up to 40MB of non-interleaved DRAM (up to 3 banks)
  - Direct DRAM drive
  - Supports base plus extension DRAM implementation (supports two device sizes in same system)
- On-chip ROM controller for up to 20MB of ROM (up to 3 banks)
  - Two-way interleaved or non-interleaved
  - Supports burst ROMs
- Programmable I/O ports provide glue-less interface to integrated low cost peripherals
  - Burst DMA interface (permits inclusion of 8530 based AppleTalk as standard feature, at lower cost than option card approach)
  - Two DMA I/O ports with on-chip 4-byte FIFO with data packing and unpacking
  - Six programmable PIO pins for peripheral interrupts
  - 8-bit and 16-bit I/O ports
- IEEE P1284 bidirectional Centronics interface supports Compatible, Nibble, Byte, ECP and EPP modes
- Coprocessor bus master DMA interface for coprocessors (e.g. Adobe's Typhoon font rasterizer)
- High performance video interface
  - Video DMA support
  - Serializer can shift right or left to support duplexing
  - On-chip 4-word x 32-bit video FIFO
  - Programmable margin counters
  - PLL with optional bypass mode
  - Video bit rates to 10 megabits per second
- General purpose functions
  - 24-bit general purpose counter/timer
- 160-pin quad plastic flatpack (PQFP)

6

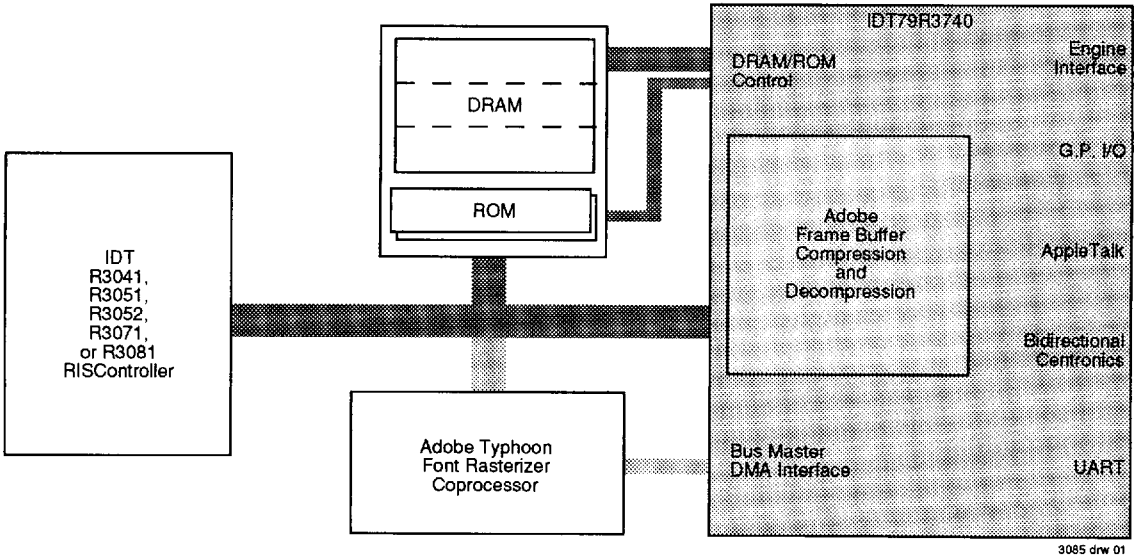


Figure 1. IDT79R3740 system organization.

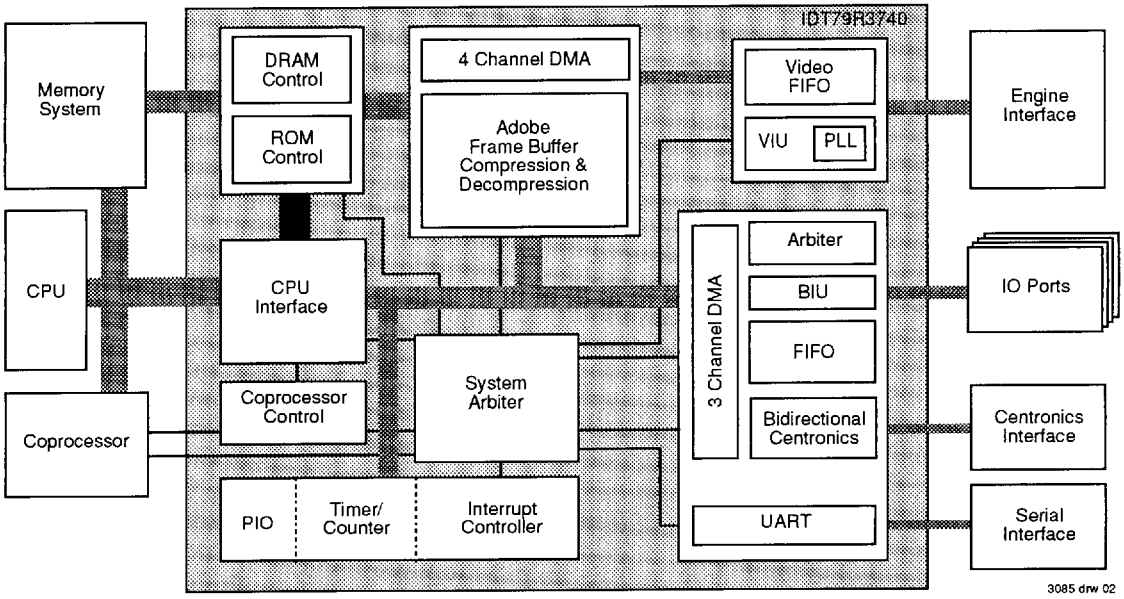


Figure 2. IDT79R3740 Block Diagram

GENERAL DESCRIPTION

The IDT79R3740 system controller is a highly integrated and programmable controller for low cost, high performance raster image systems. It utilizes Adobe Frame Buffer Compression (Adobe software accelerated by integrated hardware compression and decompression engines) to facilitate 600 dpi resolution using only 2MB of DRAM (600 dpi, 8½ x 11" printers without compression are typically implemented with 6MB of DRAM), or 3MB for implementations including both PCL5e and PostScript Level 2.

The IDT79R3740 provides direct interfaces for the R3051 family of RISControllers, a high performance, flexible memory system controller, an interface for an optional coprocessor/accelerator interface (Adobe Typhoon), a '186-like interface for industry standard I/O peripherals, and a high performance engine interface. The IDT79R3740 definition assumes that most printer OEMs want a low base unit price, with a wide range of productization options, for various cost/performance points and printing strategies.

ADOBE FRAME BUFFER COMPRESSION

Adobe provides a comprehensive solution for memory cost reduction, supporting a complex set of system goals. Two underlying printer implementation strategies are supported.

First and foremost, the compression scheme must provide greater than four-to-one compression for most of the pages printed, across a broad range of page styles, using a lossless compression algorithm to maintain high page quality, regardless of data type (fonts, graphics or scanned halftone images). This affords the opportunity to significantly lower frame buffer memory cost (by up to 4MB for a 600 dpi, 8½ x 11" page). In this model, the performance, quality and range of pages printed with full compression can be increased by adding more memory.

Secondly, Adobe Frame Buffer Compression can support a printer strategy of "printing all pages," avoiding the all-or-nothing extreme of full compression or the "page not printed because" error message. To implement this strategy, Adobe Frame Buffer Compression utilizes a two-step process, beginning with a lossless compression algorithm to provide full compression in a minimum memory system. If this cannot be achieved in the available memory space, because of overflow of the compressed buffer space, a lossy algorithm then attempts to achieve a higher compression ratio.

CPU INTERFACE

IDT79R3740 communicates with the IDT R3051 family CPUs via a multiplexed address/data bus and control interface that is a pin-for-pin, glueless match with the control signal and timing standards for IDT's RISController family, including R3041, R3051, R3052, R3071 and R3081.

A key *system* goal of IDT79R3740 is to integrate most general purpose logic to lower system cost, while preserving

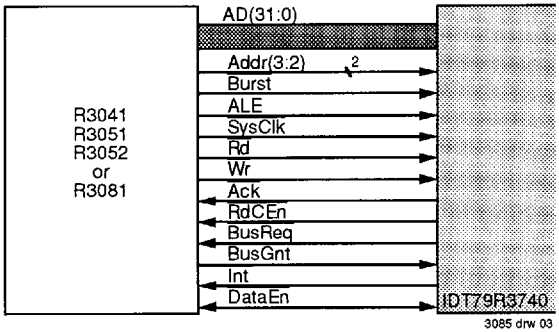


Figure 3. IDT RISController to IDT79R3740 Interface

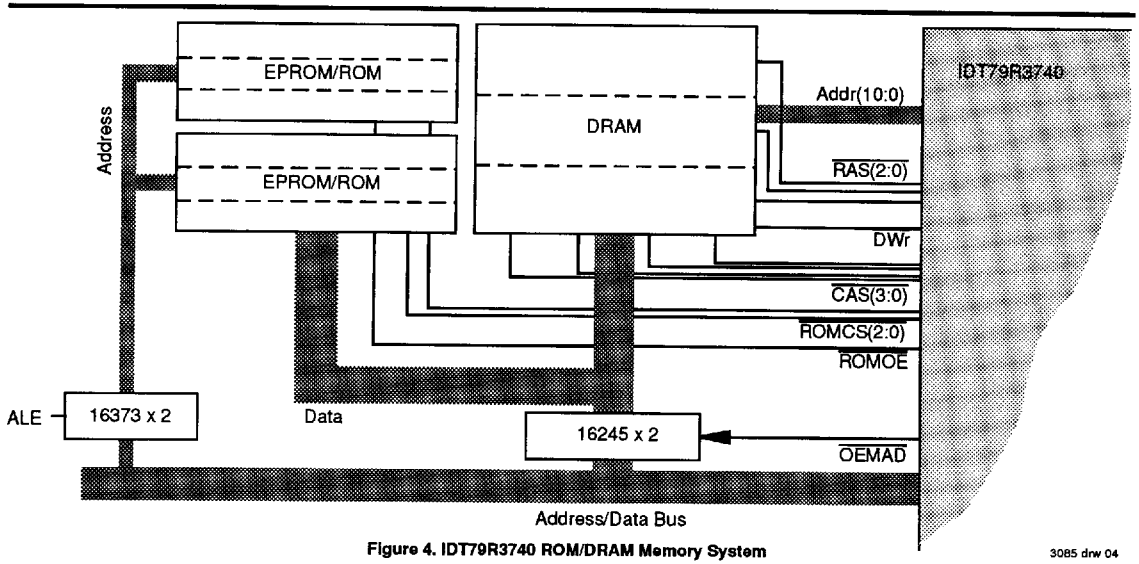


Figure 4. IDT79R3740 ROM/DRAM Memory System

3085 drw 04

OEM flexibility for product differentiation through CPU and clock frequency choices, memory timing/tuning and the addition of coprocessors.

A primary *performance* goal is to run the CPU bus at maximum utilization and frequency, with a minimum of stalls caused by memory system latencies or I/O device bandwidth limitations. IDT79R3740's on-chip FIFOs, arbitration logic and DMA capability allow I/O transfers to burst in and out of system memory at maximum memory system bandwidth. The CPU bus remains at minimum loading with only the CPU, IDT79R3740, an address latch, memory system buffers/transceivers and a system coprocessor, if used.

The IDT79R3740 provides unique system flexibility by providing programmability of the system interface functions and timing parameters. These include controls for memory configuration and device size, edge timing for DRAM and I/O peripheral control signals, and controls for the format and timing of engine interface signals. Each system interface is defined based on specific system goals for that interface. The IDT79R3740 contains Configuration Registers written during initialization, to configure the various modes, features and timing parameters.

DRAM CONTROLLER

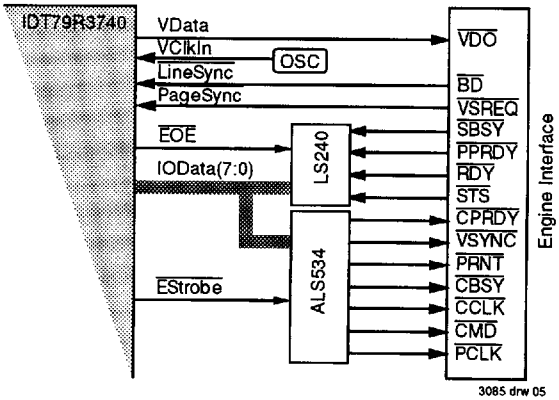
Given the low-cost goals for IDT79R3740-based systems, and the relatively low performance gain for interleaving DRAM, the R3740 provides control signals for non-interleaved DRAM. DRAM control signals support base-plus-extension 32-bit memory organizations, where the minimum DRAM configuration can be installed in the board and optional memory is added by the end user (typically standard SIMMs). Various DRAM depths are supported, and the address space is continuous for the selected configuration. The base bank ($\overline{RAS0}$) is typically different device sizes than the extension banks ($\overline{RAS1}$ and $\overline{RAS2}$).

For 33MHz systems there is an option to extend $\overline{CAS}$ by one additional cycle (also recommended for Typhoon accesses since Typhoon samples data on the rising edge of $\overline{SysClk}$, while the CPU samples data on the falling edge). The DRAM controller supports single transfer reads and writes and burst reads. DRAM device attributes supported include page mode, early write and $\overline{CAS}$-before-$\overline{RAS}$ refresh.

ROM CONTROL

The ROM controller supports up to 20MB of interleaved or non-interleaved memory. To support different system and device options, the assertion time of $\overline{RdCEn}$ and $\overline{Ack}$ can be programmed. There are three chip select lines to control up to three banks of ROM. Each bank can be either interleaved or non-interleaved. $\overline{ROMCS2}$ controls the boot bank, and has a fixed space of 4MB. The address space for $\overline{ROMCS1}$ and $\overline{ROMCS2}$ is programmable for 1, 2, 4 or 8MB. To support interleaving, a $\overline{ROMOE}$ signal is provided to control the OE of the interleave multiplexer.

The ROM controller supports burst ROMs and the capability to write to the ROM space (for flash devices or debug).



3085 drw 05

Figure 5. IDT79R3740 Engine Interface

PROGRAMMABLE ENGINE INTERFACE

The IDT79R3740 moves data from the frame buffer memory (compressed data in DRAM) to the print engine by DMA through the decompression logic for compressed bands and through decompressor bypass logic for uncompressed bands. 32-bit words are buffered in a 4-word, 32-bit wide video FIFO and serialized for output to the print engine video input. A video PLL is provided for synchronization of the video to LineSync. A PLL bypass option is provided for engines that supply the video clock.

The serializer can shift video data in either direction to support duplex printing. Also, horizontal and vertical margin counters are provided, appropriately synchronized to PageSync and LineSync.

PIO PORT AND INTERRUPT CONTROLLER

The IDT79R3740 has PIO[5:0] pins that can be individually programmed to be an input or an output. Each pin is synchronized and pulled up internally. Input pins can act as an active low interrupt. PIO(5:4) can be programmed to function as RI (Ring Indicator) and DCD (Data Carrier Detect) for the UART.

The interrupt controller serves internal resources and six external interrupts. Internal sources send a one cycle pulse that is latched by the cause register. External interrupt lines are sampled every cycle and latched by the cause register. The CPU reads the cause register to find the interrupt source. Each source is maskable via a mask register.

GLUELESS I/O CHANNELS

The IDT79R3740 supports two 8-bit and two 16-bit devices on the separate I/O Bus. CPU and Typhoon accesses are supported to I/O devices and font cartridges, as well as DMA operation between I/O devices and DRAM.

I/O channels 0-2 have 16MB address spaces and channel 3 has a 256MB address space. For 16-bit devices, the CPU can read or write to any byte or half word. CPU or Typhoon access to the 16-bit bus with all byte enables active will be performed in two successive I/O cycles. In the two cycles data will be packed or unpacked from a 32-bit register for an I/O read or write, respectively. Conversion between big and little endian is supported for 16-bit devices.

The I/O channel unit operates as a DMA controller only for slave 8-bit devices with DMA capability. 8-bit data is packed or unpacked during DMA access into a 32-bit register for I/O read and write, respectively.

The timing of control signals to an I/O device are programmable. The length of $\overline{Rd}$ and $\overline{Wr}$ can be specified. $\overline{CS}$ or $\overline{DMAAck}$ are asserted one cycle before $\overline{Rd}$ and $\overline{Wr}$ become active and remain active for one cycle after $\overline{Rd}$ and $\overline{Wr}$ are deasserted. $\overline{RdCEn}$ and $\overline{Ack}$ will be asserted by the IDT79R3740 to end a CPU or coprocessor I/O cycle.

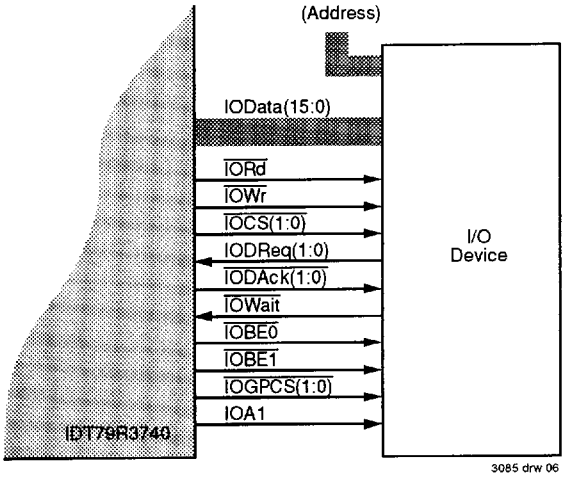


Figure 6. General Purpose I/O Device Interface

DMA APPLETALK

One of the DMA supported I/O channels can directly support AppleTalk with only the addition of the 8530 or 85230 and the I/O interface devices it requires. The IDT79R3740 's I/O FIFO and burst DMA capabilities aid in the separation of the real-time demands of the AppleTalk protocol from the real-time demands of the engine interface, without the system cost implications of "buffered AppleTalk."

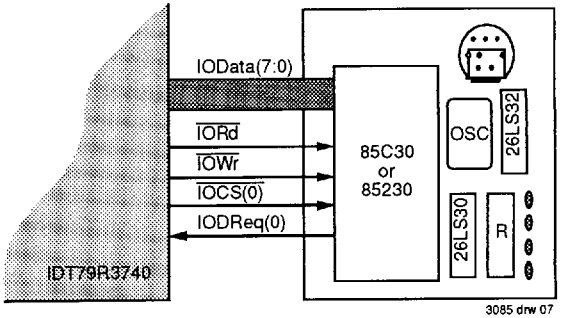


Figure 7. DMA Supported AppleTalk I/O Port

IEEE P1284 COMMUNICATION

The Centronics interface meets the IEEE P1284 definition for a compliant device.

The modes supported include: Compatible, Nibble, Byte, ECP and EPP, including the negotiating necessary for transition between different modes. Compatible mode support includes the variations: Standard, IBM Epson and Classic.

Data transfer in Compatible mode can be DMA or interrupt driven. Byte and Nibble modes are interrupt driven.

There is support for special character detection in the incoming data path. Control characters like ^C and ^T can be detected to provide a CPU interrupt.

PROGRAMMABLE TIMER/COUNTER

An internal general purpose 24-bit timer/counter is provided. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will restart the counter if the Enable bit is active.

As a timer, terminal count will cause an interrupt, reload with the value stored in the T/C Value Register and continue counting.

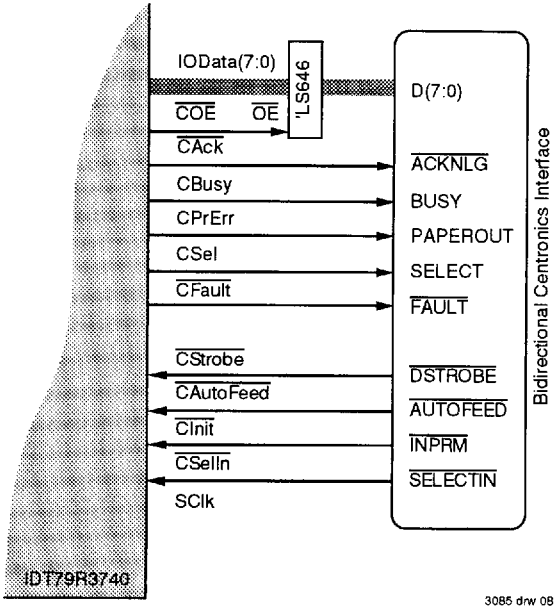


Figure 8. IEEE P1284 Bidirectional Centronics I/O Port

COPROCESSOR (TYPHOON) CONTROLLER

The IDT79R3740 provides a DMA control interface to Adobe's Typhoon coprocessor, supporting both master or slave modes. As a slave it supports CPU read and write accesses to Typhoon. As a master, Typhoon access to DRAM, ROM and I/O (for font cartridges) is enabled.

UART SERIAL INTERFACE

The UART in the IDT79R3740 is compatible with the 16550.

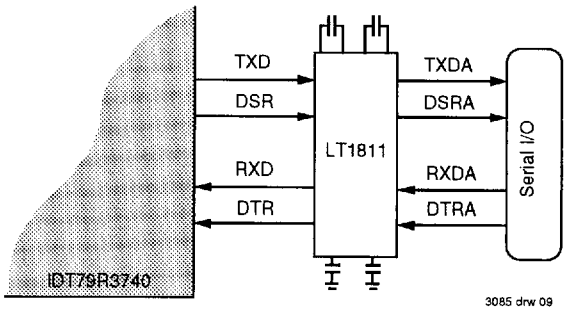


Figure 9. UART Serial Interface Implementation

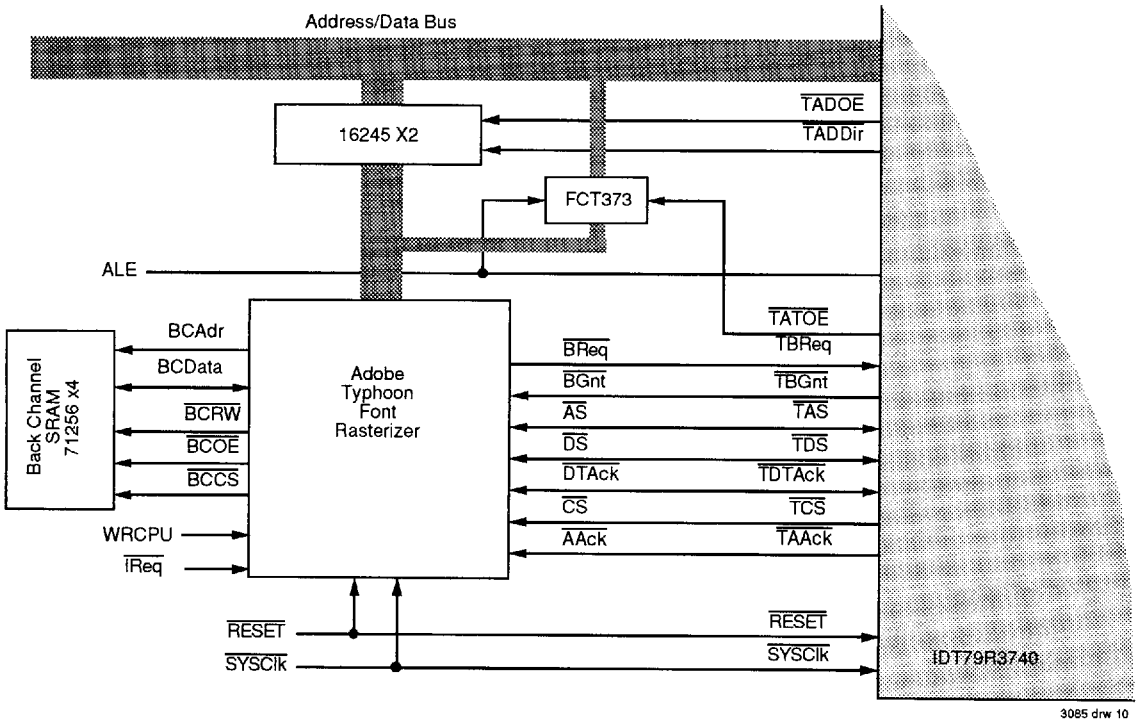


Figure 10. Adobe Typhoon Coprocessor Implementation

6