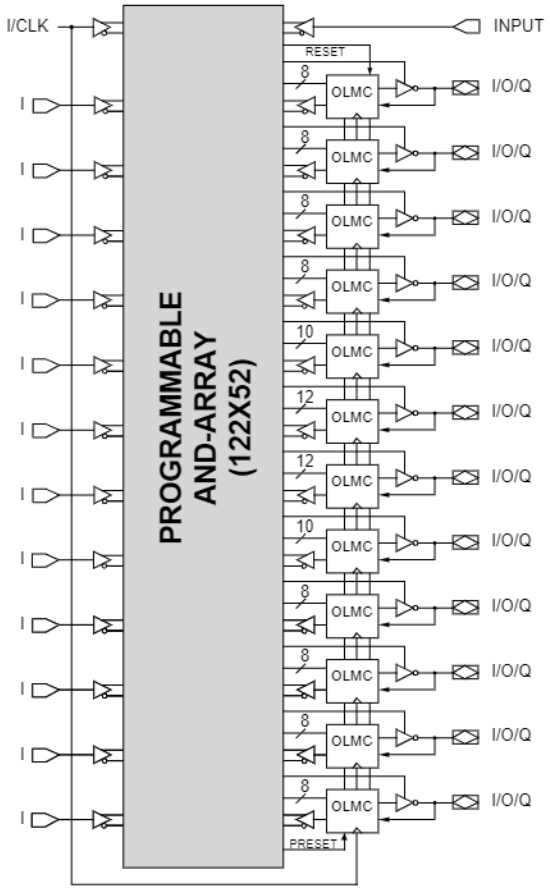
GAL26CLV12

Low Voltage E²CMOS PLD
Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 5 ns Maximum Propagation Delay
  - Fmax = 200 MHz
  - 3.5 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- **3.3V LOW VOLTAGE 26CV12 ARCHITECTURE**
  - JEDEC-Compatible 3.3V Interface Standard
  - Inputs and I/O Interface with Standard 5V TTL Devices
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **TWELVE OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - Glue Logic for 3.3V Systems
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Functional Block Diagram



Description

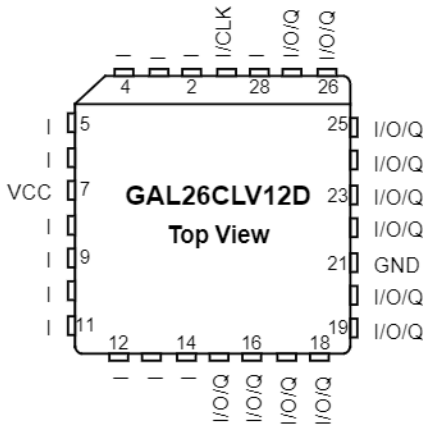
The GAL26CLV12D, at 5 ns maximum propagation delay time, provides higher performance than its 5V counterpart. The GAL26CLV12D can interface with both 3.3V and 5V signal levels. The GAL26CLV12D is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



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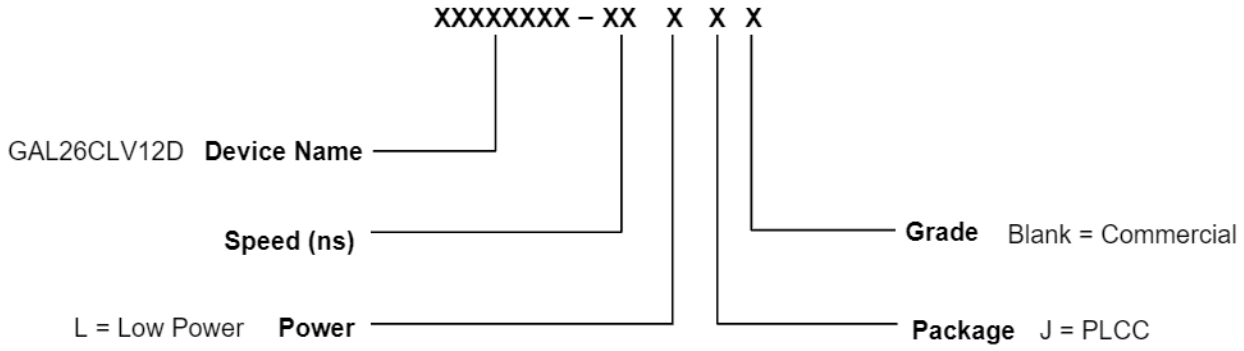
July 1997

GAL26CLV12D Ordering Information

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3.5	3.5	130	GAL26CLV12D-5LJ	28-Lead PLCC
7.5	5.5	4.5	130	GAL26CLV12D-7LJ	28-Lead PLCC

Part Number Description



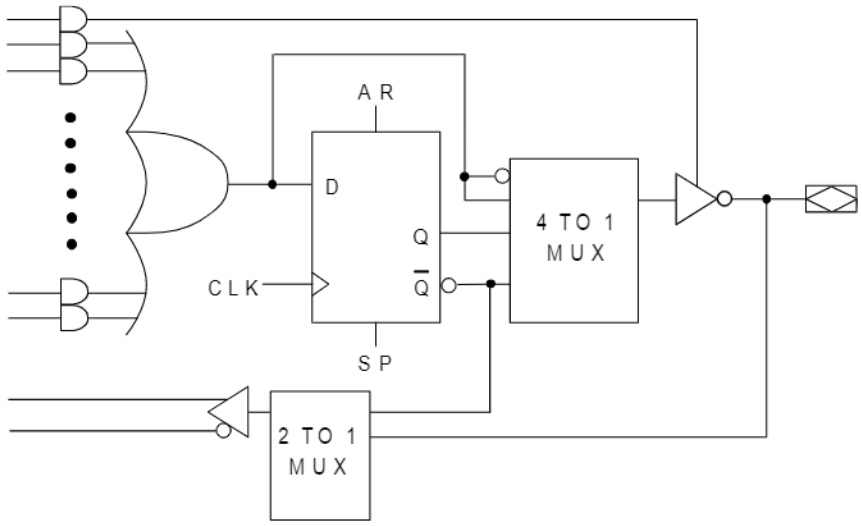
Output Logic Macrocell (OLMC)

The GAL26CLV12D has a variable number of product terms per OLMC. Of the twelve available OLMCs, two OLMCs have access to twelve product terms (pins 20 and 22), two have access to ten product terms (pins 19 and 23), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL26CLV12D has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL26CLV12D OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL26CLV12D has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (S0 and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

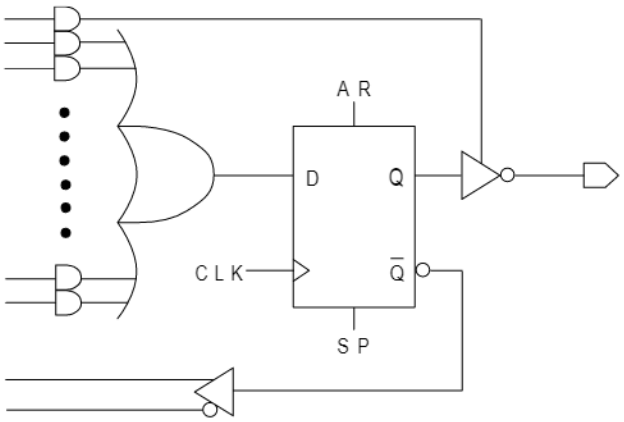
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

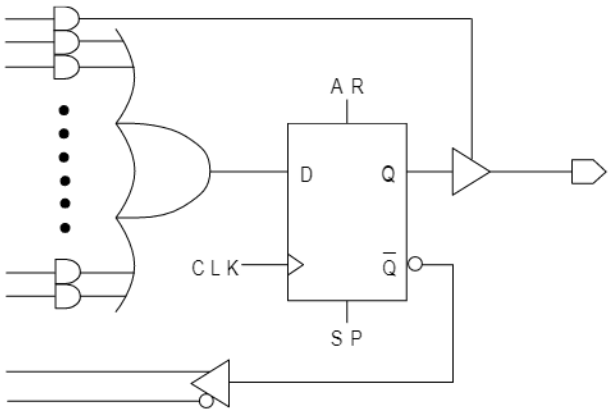
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Registered Mode



ACTIVE LOW

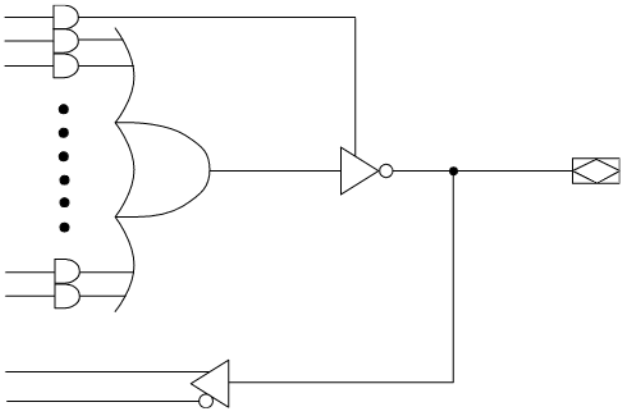
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

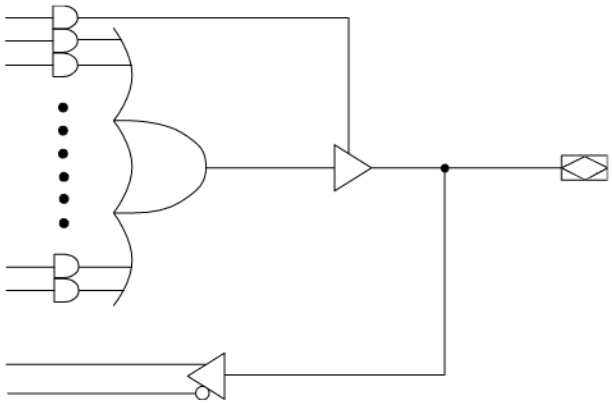
$S_0 = 1$
$S_1 = 0$

Combinatorial Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

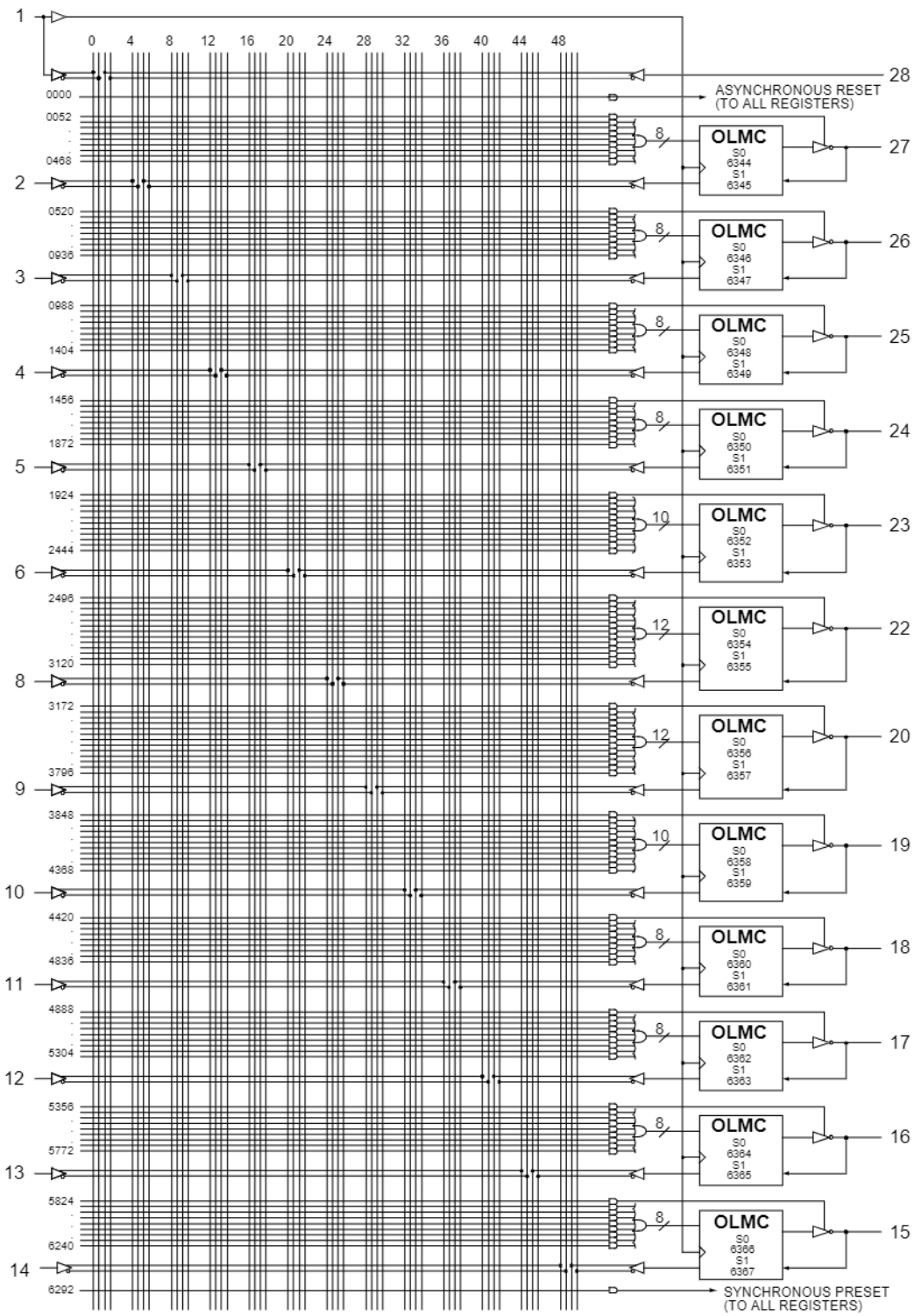


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL26CLV12D Logic Diagram/JEDEC Fuse Map

PLCC Package Pinout



6368, 6369 ... Electronic Signature ... 6430, 6431							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... -0.5 to +4.6V
Input or I/O voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +4.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
	I/O High Voltage		2.0	—	Vcc+0.5	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC}-0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
	Input Leakage Current	$V_{CC} \le V_{IN} \le 5.25V$	—	—	10	µA
	I/O Leakage Current	$V_{CC} \le V_{IN} \le 5.25V$	—	—	2	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-15	—	-80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at GND f_{toggle} = 15MHz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

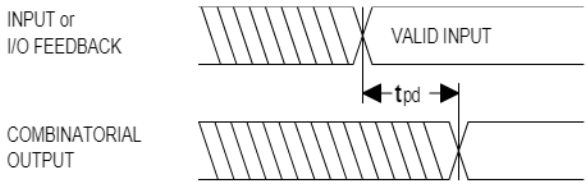
PARAMETER	TEST COND[1].	DESCRIPTION	COM -5 MIN.	COM -5 MAX.	COM -7 MIN.	COM -7 MAX.	UNITS
tpd[2]	A	Input or I/O to Combinational Output	1	5	1	7.5	ns
tco[2]	A	Clock to Output Delay	1	3.5	1	4.5	ns
tcf[3]	—	Clock to Feedback Delay	—	3	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3.5	—	5.5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	143	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	154	—	117	—	MHz
	A	Maximum Clock Frequency with No Feedback	200	—	142	—	MHz
twh[4]	—	Clock Pulse Duration, High	2.5	—	3.5	—	ns
twl[4]	—	Clock Pulse Duration, Low	2.5	—	3.5	—	ns
ten	B	Input or I/O to Output Enabled	1	6	1	7.5	ns
tdis	C	Input or I/O to Output Disabled	1	6	1	7.5	ns
tar	A	Input or I/O to Asynchronous Reset of Register	1	6	1	9	ns
tarw	—	Asynchronous Reset Pulse Duration	5.5	—	7	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	4	—	5	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	4	—	5	—	ns

1) Refer to **Switching Test Conditions** section.
2) Minimum values for **t**pd and **t**co are not 100% tested but established by characterization.
3) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
4) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

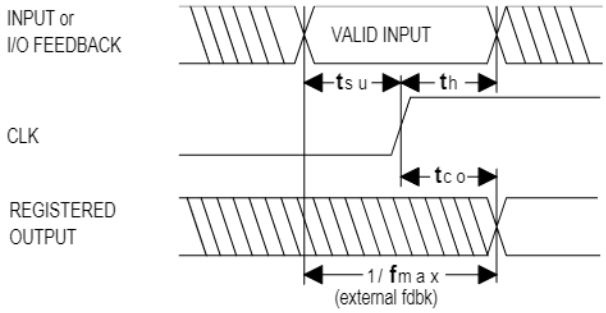
Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

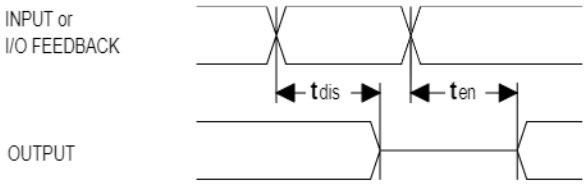
Switching Waveforms



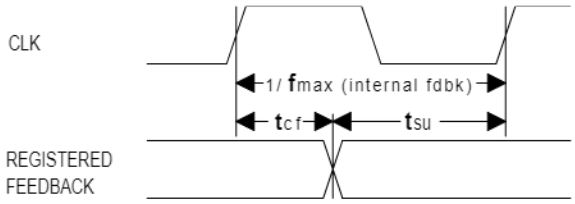
Combinatorial Output



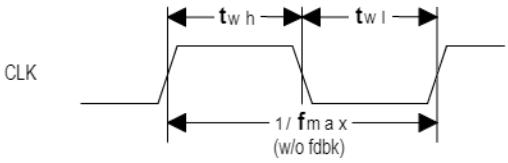
Registered Output



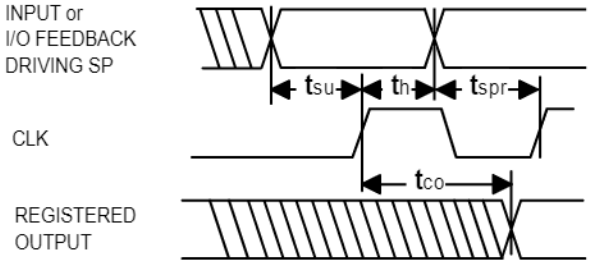
Input or I/O to Output Enable/Disable



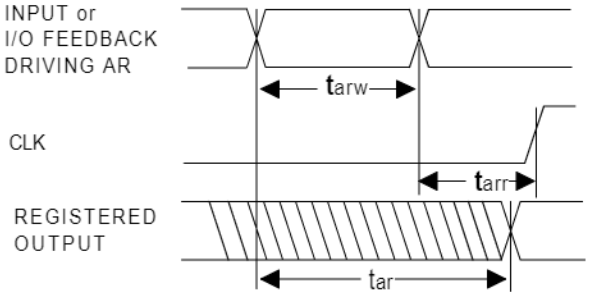
fmax with Feedback



Clock Width

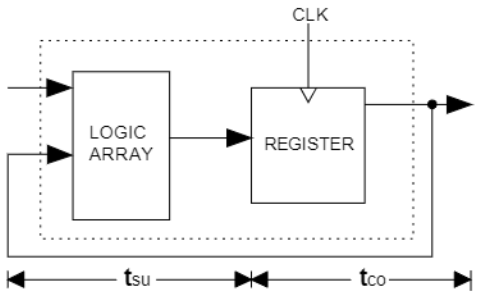


Synchronous Preset



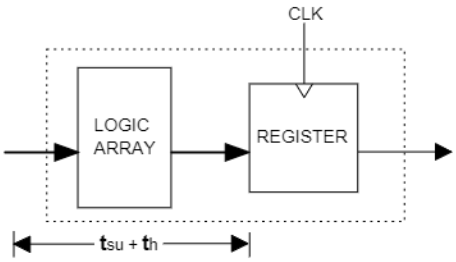
Asynchronous Reset

fmax Descriptions



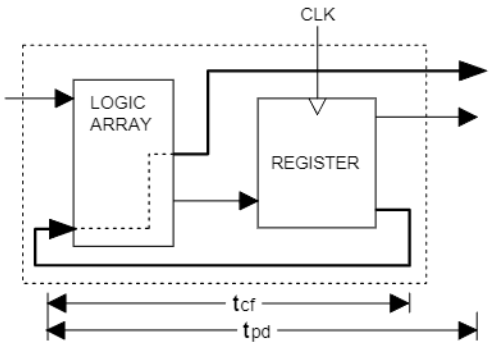
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

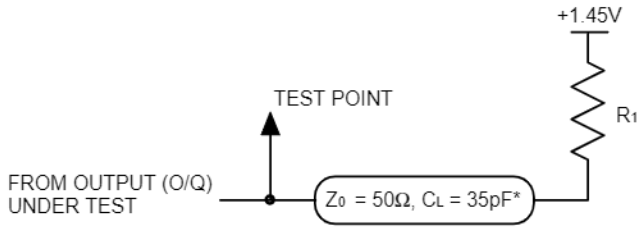
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

Electronic Signature

An electronic signature (ES) is provided in every GAL26CLV12D device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

Security Cell

A security cell is provided in every GAL26CLV12D device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL26CLV12D devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

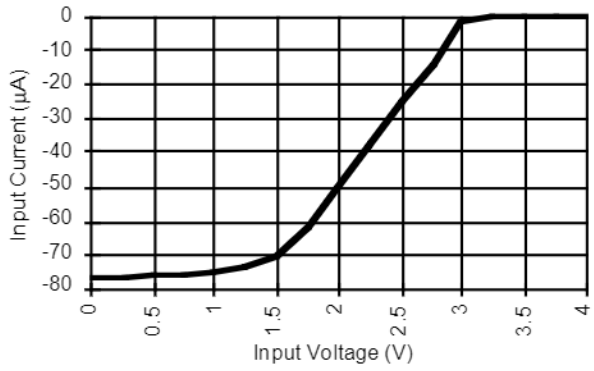
The GAL26CLV12D device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

Input Buffers

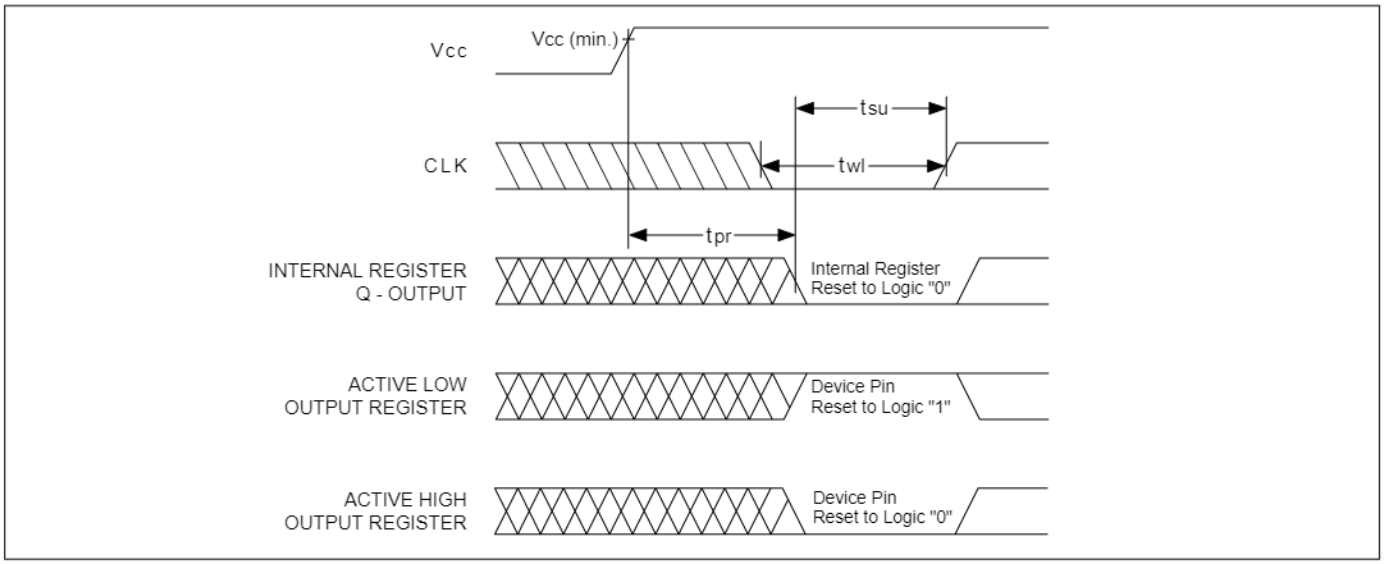
GAL26CLV12D devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins on the GAL26CLV12D also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Pull-up Characteristic

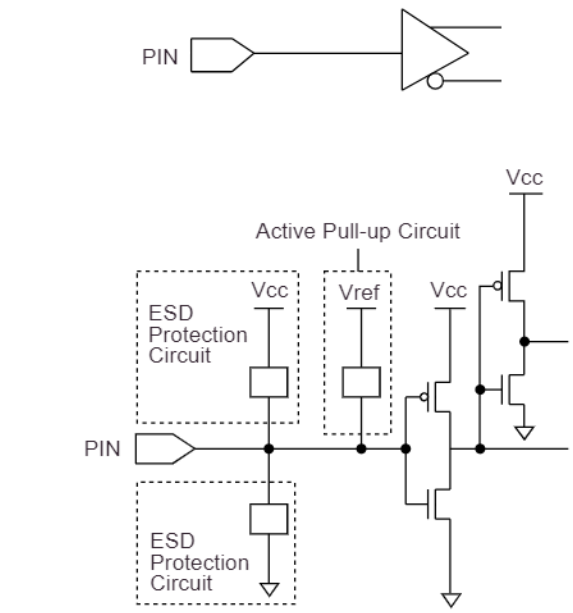


Power-Up Reset



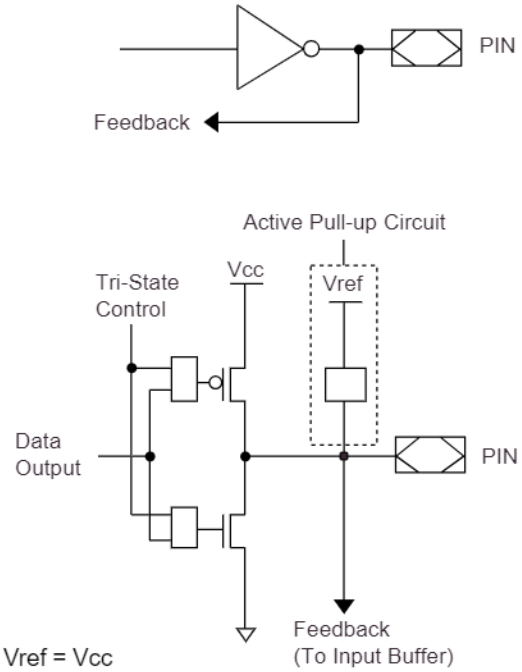
Circuitry within the GAL26CLV12D provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL26CLV12D. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Typ. Vref = Vcc

Typical Input

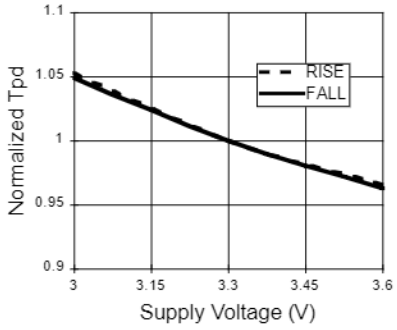


Typ. Vref = Vcc

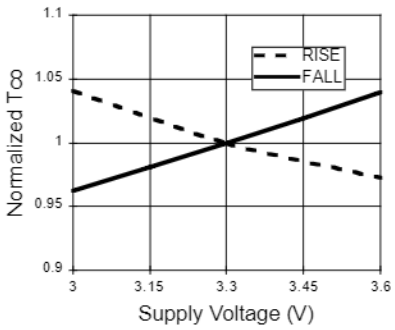
Typical Output

GAL26CLV12D: Typical AC and DC Characteristic Diagrams

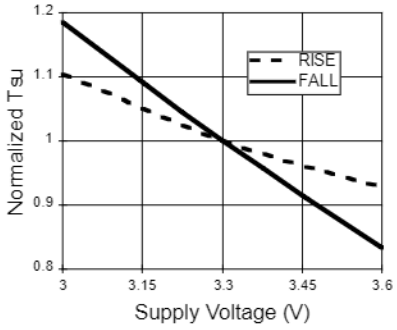
Normalized Tpd vs Vcc



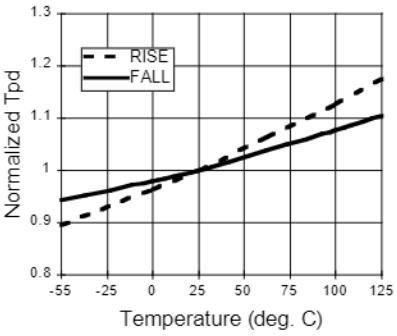
Normalized Tco vs Vcc



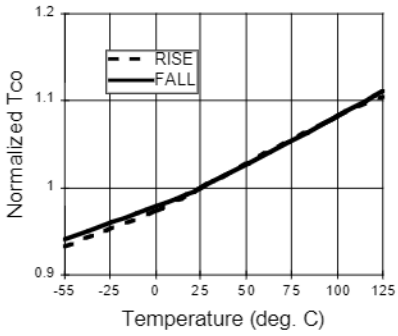
Normalized Tsu vs Vcc



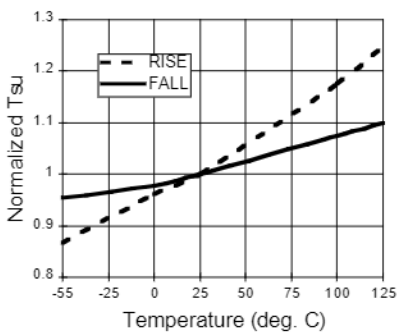
Normalized Tpd vs Temp



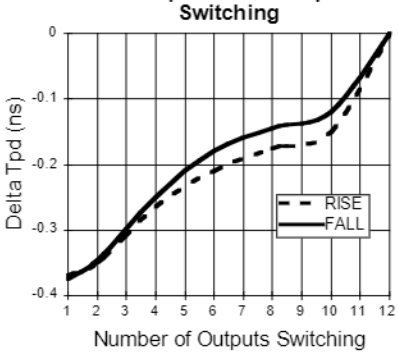
Normalized Tco vs Temp



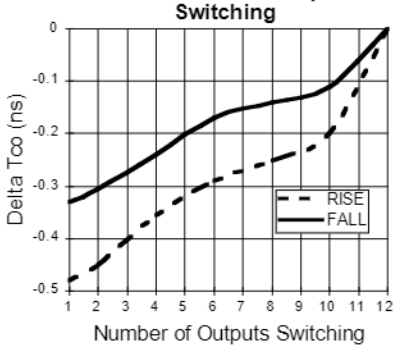
Normalized Tsu vs Temp



Delta Tpd vs # of Outputs Switching



Delta Tco vs # of Outputs Switching



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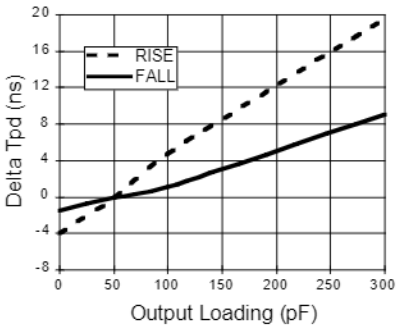
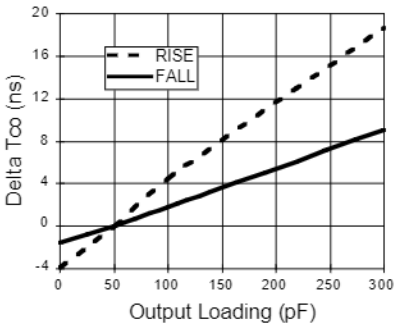
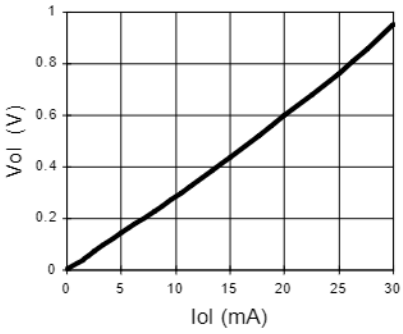


Delta Tco vs Output Loading

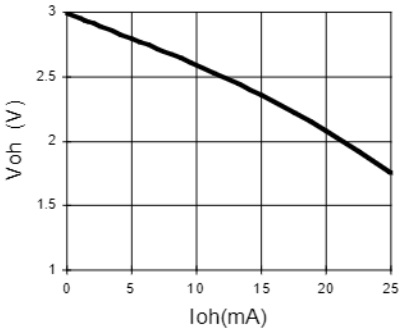


GAL26CLV12D: Typical AC and DC Characteristic Diagrams

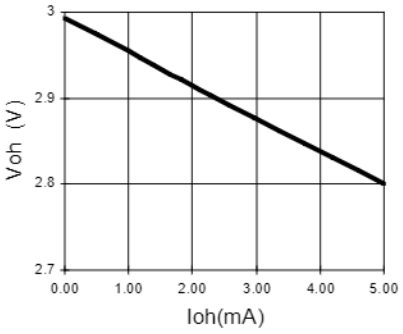
Vol vs Iol



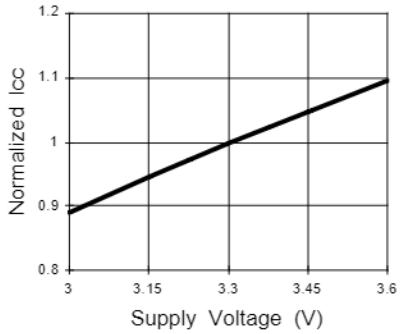
Voh vs Ioh



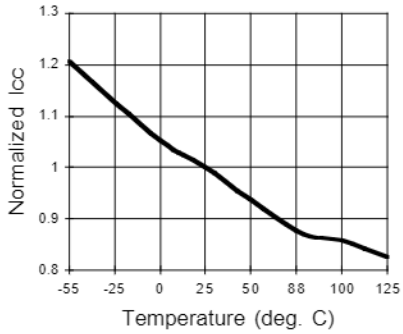
Voh vs Ioh



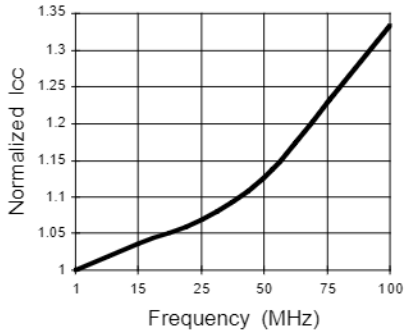
Normalized Icc vs Vcc



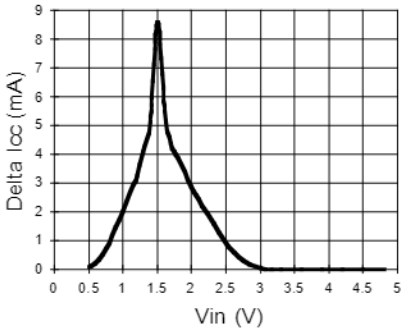
Normalized Icc vs Temp



Normalized Icc vs Freq



Delta Icc vs Vin (1 input)



Input Clamp (Vik)