TLD4012

ADSL LINE DRIVER USING TRIPATH DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information **Revision 2.0a – May 2002**

GENERAL DESCRIPTION

The TLD4012 is an ADSL line driver that provides very low power consumption and low distortion in a very small package as a result of Tripath's proprietary power processing technology. This device accepts differential input signals from an analog front-end (AFE), and can be used in full-rate (G.dmt), or G.lite systems. This TLD4012 offers a low power consumption of 650mW for full-rate, full-power, CO-side, FDM (non-overlapped) transmissions.

APPLICATIONS

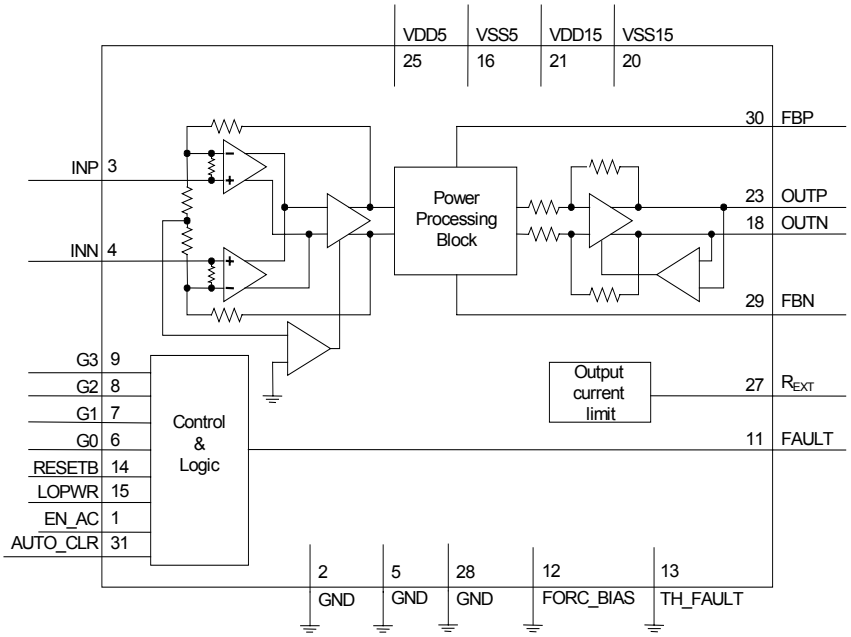
- Full-rate or G.lite line cards
- DSLAMs
- DLC equipment
- Central office switches

BENEFITS

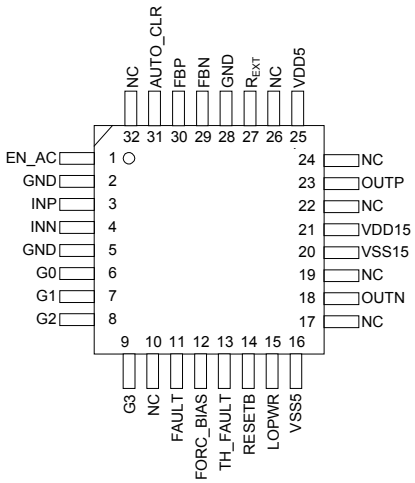
- Reduced line card power
- Reduced system power
- Increased line card density
- More ports per cubic foot of system space
- Improved system performance
- Simplifies thermal management on PCB
- Improved reliability
- Flexible solution

FEATURES

- Tripath Proprietary Power Processing technology
- Very low power consumption
- P_{CONS}(Full-rate ADSL) = 650 mW (typ)
- P_{CONS} (G.lite) = 390 mW (typ)
- Low distortion
  - Spurious free dynamic range = -80 dBc 26kHz to 138kHz, R_{LINE}=100Ω, P_{LINE}=19.8dBm
  - Third harmonic distortion = -83 dBc at f = 100 kHz, -82 dBc at f = 500 kHz, -63 dBc at f = 1 MHz, V_{OUT} = 10Vpp (differential), 70Ω load
- 500 mA minimum output current into a 71Ω load
- Digitally programmable gain (from 12.8 to 27.8 dB in 1 dB steps)
- Low-power mode -130 mW typical (line terminated -allows reception of incoming signals)
- Disabled mode - 10 mW typical (no line termination)
- Over-temperature and over-current protection with Fault output
- 5x5 mm 32-pin TQFP with exposed die pad



Block Diagram



(Top View)

OVERVIEW

TLD4012 is a low-power, low-distortion ADSL line driver. This driver offers power consumption ranging from 600mW to 650mW, and provides active, or synthetic, output impedance matching to reduce power consumption. This driver supports an impedance synthesis factor of 2.55 (refer to Figure 1 in the "Test/Applications Circuits" section of this document). The table below summarizes the total power consumption of this device for FDM and overlapped transmissions. Power consumption is reduced by using +/-14V supplies for VDD15/VSS15.

High supplies VDD15/VSS15	Power consumption FDM (non-overlapped) (19.8dBm)	Power consumption overlapped (20.4dBm)
+/- 14.0 V	650 mW	710 mW
+/- 15.0 V	675 mW	740 mW

Power consumption values given above, and in the following specifications, are for total power consumed from the supplies. This includes power dissipated in the device and power delivered to the load, where the load includes both the line and the matching resistors. Power dissipation in the driver can be determined by subtracting power delivered to the load (line and matching resistors) from the power consumption given in the specifications. The power consumption provided above does not account for loading due to the hybrid which will vary with application.

With +/-14V supplies, the maximum output swing, V_{OUTMAX}, is at least $40_{VPPDIFF}$ over process, temperature and a 5% supply tolerance. This is sufficient for full-power FDM signals with a PAR of 6.45. Note that when using +/-14V supplies with a 5% tolerance the worst-case spurious free dynamic range in the receiving band, and intermodulation distortion may be degraded slightly from the values given in the specifications below. When using 14V nominal supplies the maximum degradation expected when the +/-14V supplies are 5% low (minimum +/-13.3V) versus +/-15V supplies 5% low (minimum +/-14.25V) is less than 4dB worse case.

All other minimum and maximum specifications in the tables that follow are valid from +/-13.3 to +/-15.75V on VSS15/VDD15. This allows the use of +/-14V supplies with a 5% tolerance for VSS15/VDD15.

Lower PAR (peak-to-average ratio) values allow the high voltage supplies (VSS15 and VDD15) to be reduced further, thus reducing power consumption. For example, for a 5.3 PAR VSS15/VDD15 can be reduced to +/-12V. This will reduce power consumption to about 600mW for full-rate, 19.8dBm ADSL FDM (non-overlapped) transmissions. Contact Tripath regarding use of the TLD4012 below +/-13.3V.

The recommended values for the line-matching resistors, R_S, and the recommended transformer turns ratios to properly match the line are (see Figure 1 in "Test/Application" section below):

$R_S = 10\Omega$
N = 1:1.4

The 2.55 synthesis factor of the TLD4012 and the values above for R_S and N will result in a match to the 100Ω line impedance. The synthesis factor, k, is defined as the factor by which the line driver multiplies the line-matching resistor, R_S.

If your application can take advantage of higher synthesis factors, contact Tripath regarding options that can reduce power consumption still further.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	Value	UNITS
V_{DD5}	Positive 5V Supply Voltage	+ 6	V
V_{SS5}	Negative 5V Supply Voltage	- 6	V
V_{DD15}	Positive 15V Supply Voltage	+ 18	V
V_{SS15}	Negative 15V Supply Voltage	- 18	V
T_J	Maximum Junction Temperature	150	ºC
T_A	Operating Free-air Temperature Range	-40 to +85	ºC
T_{STORE}	Storage Temperature Range	-55 to 150	ºC
T_{SOLDER}	Manual soldering for three seconds Reflow soldering for five seconds	350 245	ºC
I_{OUT}	Output current limit, OUTP or OUTN	1.1	A
V_{IN}	Input voltage, INP or INN	V_{SS5} to V_{DD5}	V
V_{CMR}	Common mode input voltage range	V_{SS5} to V_{DD5}	V

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
2. The absolute value of VDD5 and VSS5 must always be less than or equal to the absolute value of VDD15 and VSS15.
3. **The TLD4012 incorporates an exposed die pad on the underside of its package. This acts as a heat sink and must be connected to a copper plane on the printed circuit board for proper heat dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. This copper plane must be connected to VSS15. See the Application Information section of this document for additional information.**
4. Application must insure that VSS15 is applied before VSS5. A clamp diode connected between VSS5 and VSS15 can be used to insure proper application of supply voltages to the TLD4012 (see Test/Application Circuits of this document). Note that only one diode is needed per board for multi-channel line cards, but diode selection should account for the increased current transient that the diode must carry for multiple channels. If the +/-5V rail's rise time is fast, for example in applications in which the driver's supplies might be hot-plugged, this method may not be sufficient and supply sequencing may be necessary.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD5}	Positive 5V Supply Voltage	+ 4.75	+ 5	+ 5.25	V
V_{SS5}	Negative 5V Supply Voltage	- 5.25	- 5	- 4.75	V
V_{DD15}	Positive 15V Supply Voltage	+ 13.3	+ 15	+ 15.75	V
V_{SS15}	Negative 15V Supply Voltage	- 15.75	- 15	- 13.3	V
V_{IH}	High-level Input Voltage, all digital inputs	2.7		$+V_{DD5}$	V
V_{IL}	Low-level Input Voltage, all digital inputs	0		0.8	V
I_{ODLEAK}	Open drain leakage current, FAULT output			1	µA
I_{ODMAX}	Open drain sink current at V_{OL}=0.4V max, FAULT output	1			mA

Note: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, VDD5 = +5V, VSS5 = -5V, VDD15 = +15V, VSS15 = -15V. Also, see Test/Application Circuits. See functional description for details regarding synthetic output impedance. Minimum and maximum limits are guaranteed but may not be 100% tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{CONS1}	Power Consumption	R_{LOAD} = 71Ω, P_{OUT} = 154 mW, Full-rate, overlapped ADSL signal, line power = 110 mW (20.4 dBm), with synthetic output impedance (see Fig. 1)		740		mW
P_{CONS3}	Power Consumption, no signal	R_{LOAD} = 50Ω, No Input Signal, LOPWR = Low (see Fig. 1)		250		mW
P_{CONS4}	Power Consumption, no signal, low power mode	R_{LOAD} = 50Ω, No Input Signal, LOPWR = High (see Fig. 1)		130		mW
P_{CONS5}	G.Lite	R_{LOAD} = 71Ω, P_{OUT} = 58 mW, G.Lite signal, line power = 41.6 mW (16.2 dBm). See Fig. 1.		390		mW
P_{CONS6}	Disable mode	RESETB = Low		10		mW
I_{DD5}	Operating Current VDD5	R_{LOAD} = 71Ω, P_{OUT} = 154 mW, Full-rate, overlapped ADSL signal with synthetic output impedance (see Fig. 1)		47.0		mA
I_{SS5}	Operating Current VSS5	R_{LOAD} = 71Ω, P_{OUT} = 154 mW, Full-rate, overlapped ADSL signal with synthetic output impedance (see Fig. 1)		49.0		mA
I_{DD15}	Operating Current VDD15	R_{LOAD} = 71Ω, P_{OUT} = 154 mW, Full-rate, overlapped ADSL signal with synthetic output impedance (see Fig. 1)		8.0		mA
I_{SS15}	Operating Current VSS15	R_{LOAD} = 71Ω, P_{OUT} = 154 mW, Full-rate, overlapped ADSL signal with synthetic output impedance (see Fig. 1)		9.5		mA
I_{q1}	Quiescent Current (VDD5 and VSS5)	R_{LOAD} = 71Ω, No input signal, LOPWR = Low		21.7		mA
I_{q2}	Quiescent Current (VDD15 and VSS15)	R_{LOAD} = 71Ω, No input signal, LOPWR = Low		1.1		mA
I_{q1LP}	Quiescent Current (VDD5 and VSS5), low power mode	R_{LOAD} = 71Ω, No input signal, LOPWR = High		11.0		mA
I_{q2LP}	Quiescent Current (VDD15 and VSS15), low power mode	R_{LOAD} = 71Ω, No input signal, LOPWR = High		0.68		mA
V_{BG}	Band-gap Voltage			1.28		V
V_{OUTmax}	Differential Output Voltage, peak-to-peak differential	Gain = 17.8 to 27.8 dB, R_{LOAD} = 71Ω Gain = 12.8 to 16.8 dB, R_{LOAD} = 71Ω	42 20			V
I_{OUTmax}	Differential Output Current	R_{LOAD} = 71Ω	500			mA
I_{SC}	Short-circuit Output Current	R_{EXT} = 24kΩ		800		mA
V_{IO}	Differential Input Offset Voltage			600		μV
ΔV_{OS}	Offset Voltage Drift			30		μV/°C
V_{OSHI}	Differential Output Offset Voltage	Gain = 27.8dB, EN_AC = High, 5kΩ across INN and INP	-100		100	mV
I_b	Input Bias Current	EN_AC = Low		0.5		μA
ΔI_b	Differential Input Bias Current			0.2		μA
R_{IDIFF}	Differential Input Resistance			800		kΩ
C_{IDIFF}	Differential Input Capacitance			2		pF
R_{OUTLP}	Output Resistance (while in Low-power mode)	LOPWR = High		0.5		Ω

PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, VDD5 = +5V, VSS5 = -5V, VDD15 = +15V, VSS15 = -15V. Also, see Test/Application Circuit. Minimum and maximum limits are guaranteed but may not be 100% tested.

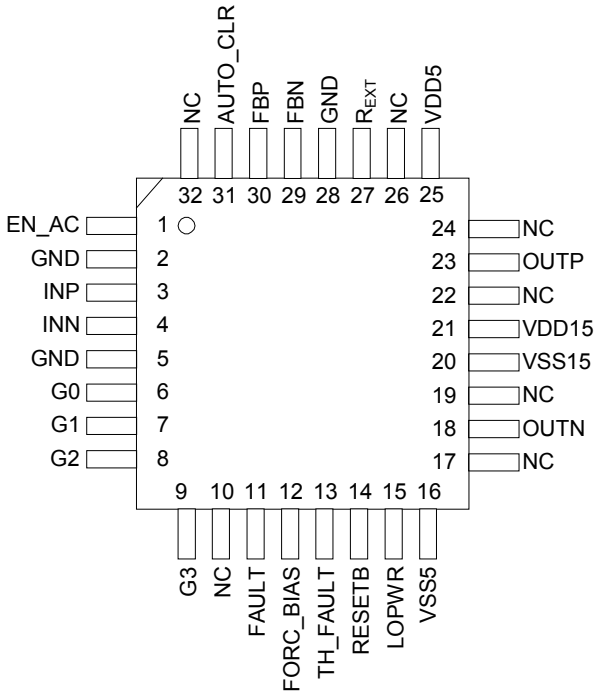
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
BW_{SS}	Small-signal Bandwidth, -3 dB	Gain = 20.8dB, V_{OUT} = $1V_{PPDIFF}$			10		MHz
SFDR	Spurious Free Dynamic Range in the receive band with respect to –40dBm ADSL transmit signal	Gain = 20.8 dB, R_{LINE} = 100Ω, P_{LINE} = 20.4 dBm, f = 26 kHz to 138 kHz			-80		dB
IMD	Intermodulation Distortion	Gain = 22.8dB $10V_{PPDIFF}$ each tone f = 1.025MHz, Δf = 50kHz	@ 50 kHz @ 100 kHz SFDR >1MHz		-84 -84 -75		dBc
HD2	2nd Harmonic Distortion	Gain = 17.8 to 27.8dB R_{LOAD} = 71Ω V_{OUT} = $10V_{PPDIFF}$	f = 100 kHz f = 500 kHz f = 1 MHz		-90 -77 -70		dBc
HD3	3rd Harmonic Distortion	Gain = 17.8 to 27.8dB R_{LOAD} = 71Ω V_{OUT} = $10V_{PPDIFF}$	f = 100 kHz f = 500 kHz f = 1 MHz		-83 -82 -63		dBc
HD5	5th Harmonic Distortion	Gain = 17.8 to 27.8dB R_{LOAD} = 71Ω V_{OUT} = $10V_{PPDIFF}$	f = 100 kHz f = 500 kHz f = 1 MHz		-93 -67 -55		dBc
SR	Slew Rate	VOUT from –10V to +10V, measured from –7.5V to +7.5V, Gain = 20.8 dB			200		V/µs
e_N	Input Noise Voltage	Gain = 20.8dB, f = 10 KHz			8		nV/ √Hz
i_N	Input Noise Current	Gain = 20.8dB, f = 10 kHz			2.9		pA/ √Hz
e_{NOTOT}	Overall Output Noise Voltage	Gain = 20.8dB, f = 30kHz to 1.1MHz, R_{IN} = 5kΩ			188		nV/ √Hz
CMRR	Common Mode Rejection Ratio	Gain = 27.8 dB V_{IN} = 100 mV_{PP} EN_AC = High	@ 100 kHz @ 500 kHz @ 1 MHz	65	83 70 65		dB
$PSRR_{VDD5}$	Power Supply Rejection Ratio, VDD5	Gain = 22.8 dB $V_{SUPPLYAC}$ = 100 mV_{PP}	@ 100 kHz @ 500 kHz @ 1 MHz		70 60 50		dB
$PSRR_{VSS5}$	Power Supply Rejection Ratio, VSS5	Gain = 22.8 dB $V_{SUPPLYAC}$ = 100 mV_{PP}	@ 100 kHz @ 500 kHz @ 1 MHz		60 52 45		dB
$PSRR_{VDD15}$	Power Supply Rejection Ratio, VDD15	Gain = 22.8 dB $V_{SUPPYAC}$ = 100 mV_{PP}	@ 100 kHz @ 500 kHz @ 1 MHz		82 76 67		dB
$PSRR_{VSS15}$	Power Supply Rejection Ratio, VSS15	Gain = 22.8 dB $V_{SUPPLYAC}$ = 100 mV_{PP}	@ 100 kHz @ 500 kHz @ 1 MHz		75 59 51		dB
ΔGain	Gain accuracy	Output=$TBDV_{PPDIFF}$, 500kHz		-0.4		0.4	dB

PIN DESCRIPTION

PIN	PIN NAME	PIN FUNCTION	PIN DESCRIPTION
1	EN_AC	Digital input	A logic high enables the input common-mode feedback loop, and input bias current cancellation circuit
2	GND	Ground	Device Ground
3	INP	Analog input	Positive terminal of differential input
4	INN	Analog input	Negative terminal of differential input
5	GND	Ground	Device Ground
6	G0	Digital input	Least Significant Bit of programmable gain select
7	G1	Digital input	Second Least Significant Bit of programmable gain select
8	G2	Digital input	Third Least Significant Bit of programmable gain select
9	G3	Digital input	Most Significant Bit of programmable gain select
10	NC	No Connect	
11	FAULT	Digital output (open drain)	A logic level high indicates that the device has an output short circuit or that a thermal overload has occurred
12	FORC_BIAS	Digital input	When set to a logic high, the device forces the bias on regardless of fault conditions Intended for test only
13	TH_FAULT	Analog input	When set to a logic high, the device simulates a thermal fault. Intended for test only
14	RESETB	Digital input	When AUTO_CLR is set to a logic low, a logic low pulse on RESETB clears the internal Fault latch; otherwise, connect RESETB to VDD5; Logic low puts device in disabled mode
15	LOPWR	Digital input	When set to logic high, the device goes into low-power mode
16	VSS5	Power supply	Negative 5V supply voltage
17	NC	No Connect	
18	OUTN	Analog output	Negative terminal of differential output
19	NC	No Connect	
20	VSS15	Power supply	Negative 15V supply voltage
21	VDD15	Power supply	Positive 15V supply voltage
22	NC	No Connect	
23	OUTP	Analog output	Positive terminal of differential output
24	NC	No Connect	
25	VDD5	Power supply	Positive 5V supply voltage
26	NC	No Connect	
27	R_{EXT}	Analog input	Sets over-current limit
28	GND	Ground	Device Ground
29	FBN	Analog input	Feedback path for synthesized output impedance
30	FBP	Analog input	Feedback path for synthesized output impedance
31	AUTO_CLR	Digital input	A logic high forces an immediate reset of the fault latch when RESETB is a logic high. A logic low requires that the RESETB pin be pulsed low to reset the fault latch
32	NC	No Connect	
EP	Exposed pad	Substrate	Exposed pad at underside of device; must be connected to VSS15. Internally connected to the substrate.

TLD4012
32-PIN TQFP WITH EXPOSED DIE PAD

(Top View)



FUNCTIONAL DESCRIPTION

Programmable Gain

The gain of the TLD4012 is programmed by the digital inputs G3, G2, G1 and G0. The gain given below is the gain from the input to the output of the TLD4012 with R_S=10Ω and R_{LOAD}=50Ω as shown in Figure 1. Note that output voltage swing is limited for gains less than 17.8 dB (see parameter V_{OUTMAX} in Electrical Characteristics).

G3	G2	G1	G0	Gain, dB	Gain, V/V
0	0	0	0	12.8	4.37
0	0	0	1	13.8	4.90
0	0	1	0	14.8	5.50
0	0	1	1	15.8	6.17
0	1	0	0	16.8	6.92
0	1	0	1	17.8	7.76
0	1	1	0	18.8	8.71
0	1	1	1	19.8	9.77
1	0	0	0	20.8	10.96
1	0	0	1	21.8	12.30
1	0	1	0	22.8	13.80
1	0	1	1	23.8	15.49
1	1	0	0	24.8	17.38
1	1	0	1	25.8	19.50
1	1	1	0	26.8	21.88
1	1	1	1	27.8	24.55

Protection Circuits

The TLD4012 has built-in protection against over-temperature and over-current conditions. There are two modes in which the fault protection circuits can operate depending on the state of the AUTO_CLR pin. The two modes operate as follows:

1. AUTO_CLR pin is set to a logic low level - When the device goes into an over-temperature or over-current condition, the FAULT pin is latched into a logic HIGH state indicating a fault condition. When this occurs, the amplifier outputs enter disable mode and are in a high-impedance state provided OUTP and OUTN are not driven externally to exceed approximately +/-2.0V_{ppdiff}. After the fault condition has been removed, a logic LOW pulse must be applied to the RESETB pin for a minimum of 100 ns to reset the FAULT output to a logic low level, and re-enable the output to a normal, low impedance mode.
2. AUTO_CLR pin is set to a logic high level - After a fault occurs and the fault condition is removed, the device will enable the outputs, and reset the FAULT pin every 1 micro-second. In this mode the fault latch is reset internally on power up so an external reset is not required. Note that in the case of an over-current fault, if the cause of the over-current condition has not actually cleared, the output stage will cycle continuously between the normal, enabled state, and the fault, or disabled state. In this mode the FAULT output pin can cycle continuously until the cause of the fault is cleared. If this operation is not desirable, see the “Over-current Protection” section below. If a microcontroller or DMT processor is used to monitor the FAULT output, and to control the device, AUTO_CLR should be set to a logic low level. Otherwise, AUTO_CLR should be set to a logic high level and the device will reset itself on power-up and after a fault condition has been removed.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the device exceeds approximately 160°C. When a fault occurs the TLD4012 output driver enters the disabled mode, and asserts a logic HIGH on the FAULT pin. An over-temperature fault can only be cleared after the junction temperature drops below approximately 120°C.

Over-current Protection

An over-current fault occurs when current delivered from either of the output pins, OUTP or OUTN, exceeds the current limit value. When a fault occurs, the TLD4012's output driver enters disabled mode, and asserts a logic HIGH on the FAULT pin. The level at which the current limit occurs is set by R_{EXT}. The relationship between the over-current limit and R_{EXT} is:

R_{EXT} = 19.2 / I_{CL} , where I_{CL} is the short circuit current limit in A, and R_{EXT} is in kΩ.

The acceptable range of R_{EXT} is 19.2 kΩ to 32 kΩ, or 1.0 A to 600 mA, respectively. A typical value for R_{EXT} in most ADSL applications is 24kΩ which results in an 800mA current limit.

If the device is operated with AUTO_CLR set to a logic high level, and an over-current condition occurs, the device will cycle between the fault state and normal state as described in the "Protection Circuits" section above.

If the cycling mode described above is not desirable, the over-current limit can be set to 1.0 A, (i.e. R_{EXT} = 19.2 kΩ). With this current limit value, the device will not enter the cycling mode if a short occurs on the twisted pair because the matching resistors, R_S, will limit the current to less than 1.0A. The over-temperature protection will eventually act to protect the device, and in the event of a short on the board, the over-current protection will still take affect to protect the device.

Low-Power Mode

The TLD4012 can be placed into a low-power consumption mode by asserting a logic HIGH on the LOPWR input. In this mode the device consumes approximately 130 mW, but still provides a low output resistance to allow reception of incoming signals.

Disable Mode

The TLD4012 can be placed in a lower power disabled mode by holding RESETB to a logic low level. In this mode the power dissipation is only 10 mW, and the line is not terminated so reception of incoming signals is not reliable. In this mode the outputs are high impedance as long as they are not driven externally more than about +/-2.0V_{ppdiff} around ground. Beyond this voltage the outputs become low impedance.

Upon power-up the TLD4012 does not exit disabled mode until the VDD5/VSS5 power supply pins are greater than about 4.2V. It will automatically enter disabled mode when the VDD5/VSS5 supply pins are less than about 4.0V.

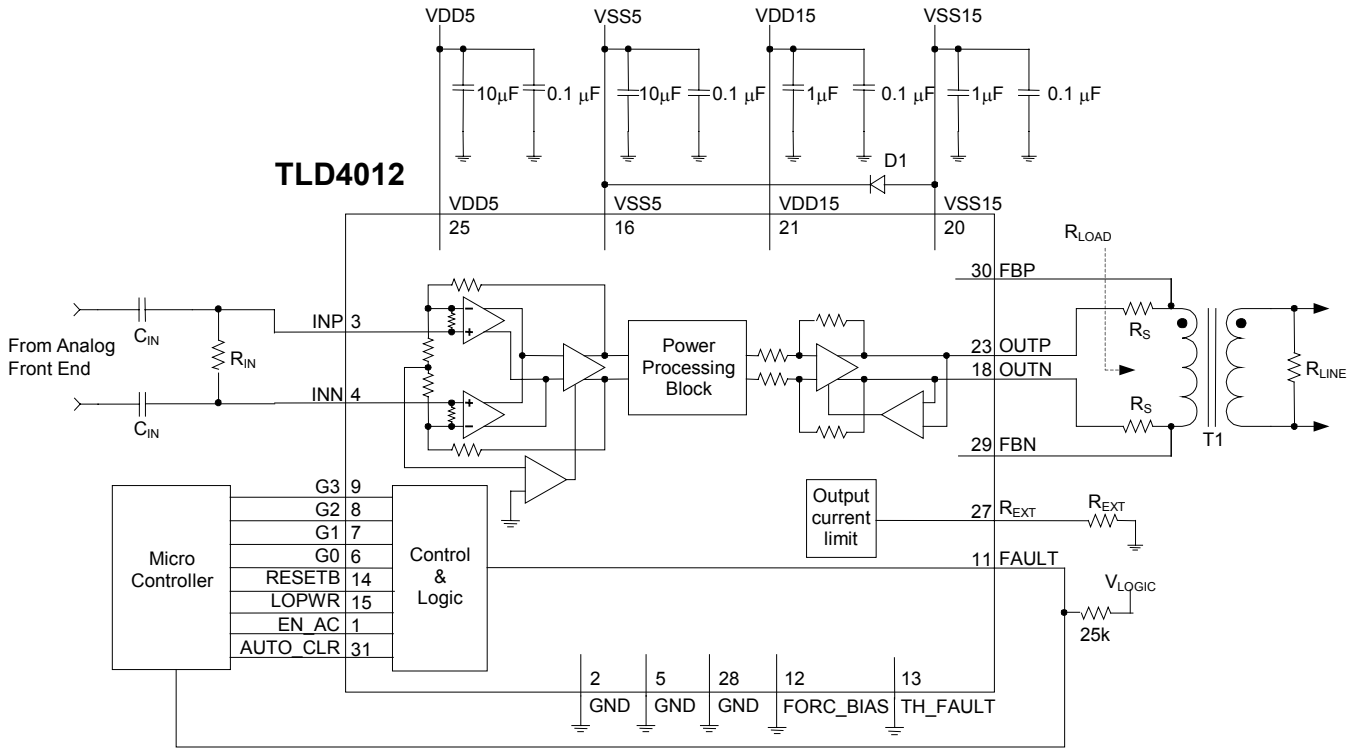
Input Common-mode Feedback Loop and Input-Bias-Current Cancellation

The TLD4012 has a common-mode feedback loop on the input stage and an input-bias-current cancellation circuit. Setting the EN_AC input to a logic high level enables both features. When enabled the common-mode feedback loop will set the common-mode input voltage. This allows use of a differential filter (i.e. not referenced to ground) between the AFE and the driver. When the common-mode feedback loop is disabled (EN_AC = Low) the application should replace the single input resistor, R_{IN}, shown in Figure 1 with two input resistors connected from the inputs, INN and INP, to ground.

TEST/APPLICATION CIRCUIT

Synthesized Output Impedance

Device TLD4012 employs synthesized output impedance with a synthesis factor of 2.55. As with any line driver, using synthesized impedance reduces power consumption, but may compromise receive-signal strength in some applications. The 10Ω matching resistors will properly terminate a 100Ω line when a 1:1.4 transformer is used (see Figure 1). Note that, for simplicity, the hybrid and other filtering associated with the receive signal path are not shown.



T1 = 1:1.4 Transformer
C_{IN} = 0.1 µF
R_{IN} = 5 kΩ
R_S = 10 Ω
R_{EXT} = 24 KΩ
R_{LINE} = 100 Ω
D1 = One UPS840 schottky diode or equivalent per 48 drivers.

Test/Application Circuit – with synthesized output impedance, TLD4012

Figure 1

APPLICATION INFORMATION

Power Dissipation Derating for 5x5mm TQFP with Exposed Die Pad

For operating at ambient temperatures above 25°C the device power dissipation, $P_{DISS,}$ must be de-rated based on a 150°C maximum junction temperature T_J (max) as given by the following equation:

$$P_{DISS} = (T_J(max) - T_A)/\theta_{JA}$$

Where θ_{JA} of the package is determined from the table, and T_A is the ambient temperature.

Airflow (LFPM)	θ_{JA},C/W (Copper Pad Soldered To PCB)
	5x5mm
0	34.5
200	29.1
500	27.2

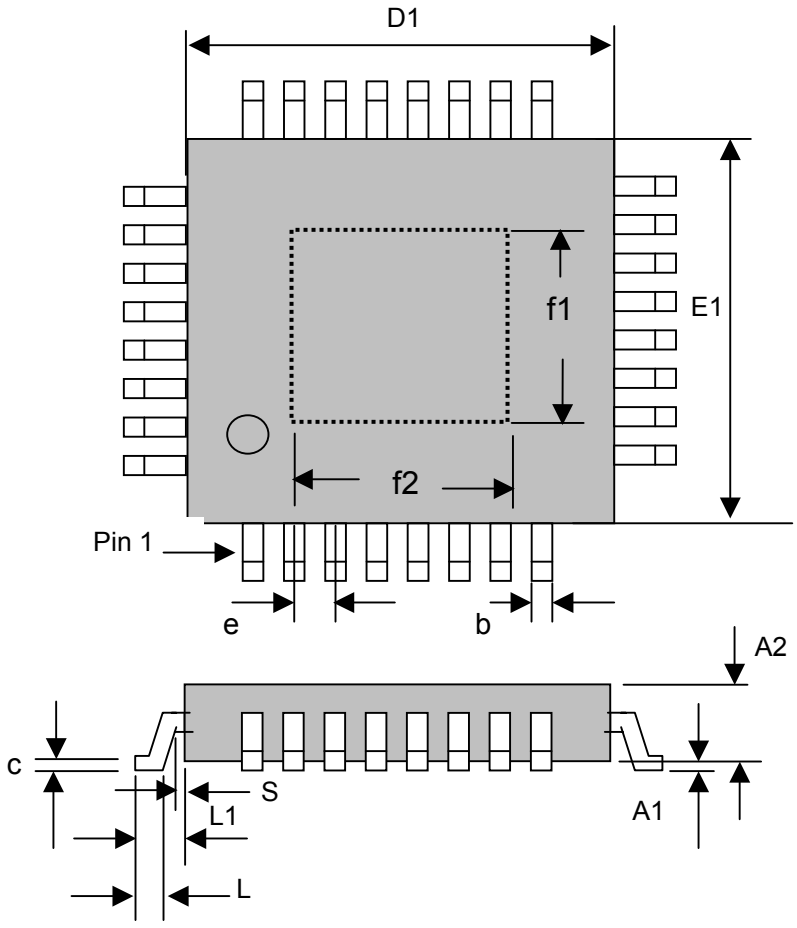
Values apply when the exposed pad is soldered to a JEDEC standard test board.

Note that P_{DISS} is the power dissipated on the chip, not P_{CONS} which is the power consumed from the supplies.

The TLD4012 incorporates an exposed die pad on the underside of its package. This acts as a heat sink and should be connected to a copper plane on the printed circuit board for optimum heat dissipation. This copper plane must be connected to VSS15.

PACKAGE INFORMATION

5x5mm TQFP with exposed die pad



All dimensions in mm

BODY SIZE		LEAD COUNT	STAND-OFF	BODY THICKNESS	LEAD LENGTH	LEAD WIDTH	LEAD THICKNESS	LEAD PITCH	LEAD BOTTOM ATTACH	LEAD SHOULDER	EXPOSED PAD (BOTTOM SIDE)	
D1	E1		A1	A2	L1	b	c	e	L	S	f1	f2
5.0	5.0	32	0.04	1.0	1.0	0.22	0.15	0.5	0.45-0.75	Min0.2	3.5	3.5

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