DATA SHEET

SUNPLUS

SPLC086A

80ch Common/Segment Driver for Dot Matrix LCD

NOV. 03, 2004

Version 1.0

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80CH COMMON/SEGMENT DRIVER FOR DOT MATRIX LCD

1. GENERAL DESCRIPTION

The SPLC086A is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

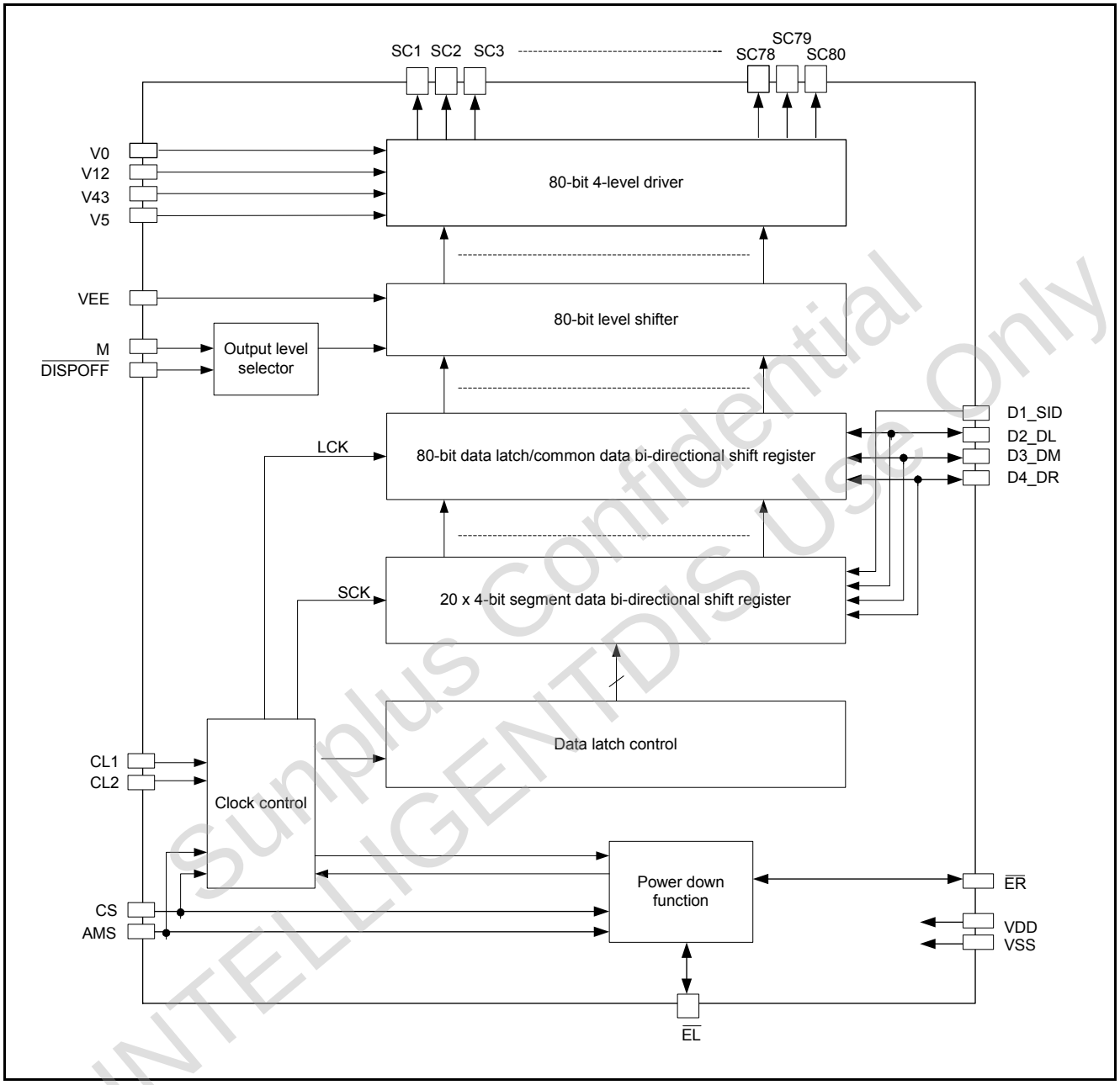
2. FEATURES

- Power supply voltage: +5.0V ± 10 %, +3.0V ± 10%
- Supply voltage for display: 6.0V to 28V (VDD-VEE)
- 4-bit parallel/1-bit serial data processing (in segment mode)
- Single mode operation/dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD Duty: 1/64 – 1/256
- Interface

Drivers	
COM (cascade)	**SEG (cascade)**
SPLC086A	SPLC086A

- High voltage CMOS process
- Available PKG type: bare die, 100 LQFP

3. BLOCK DIAGRAM



3.1. Block Descriptions

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin ($\overline{EL}$ or $\overline{ER}$). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and $\overline{DISPOFF}$) (refer to ***4.SIGNAL DESCRIPTIONS***).	COM/SEG
20x4-bit segment data bi-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch/ common data bi-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to ***4.4 Data Shift Direction According to Control Signals***).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. And when in common driver application, this value becomes V1 or V4.	COM/SEG

4. SIGNAL DESCRIPTIONS

Mnemonic	Input/ Output	Name	Function	Interface
VDD			Logical "High" input port (+5.0V ± 10%, +3.0V ± 10%)	Power
VSS			0V (GND) **add "add a resistor(10ohm) to resist power bounce."**	
VEE			Logical "Low" for high voltage part **add "add a resistor(10ohm) to resist power bounce."**	
V0, V12 V43, V5	Input	LCD driver output voltage level	Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to ***4.3***).	Power
SC1 - SC80	Output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to ***4.1 Output level control***).	LCD
CL2	Input	Data shift clock	Clock pulse input for the bi-directional shift register. 1). In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift register at the falling edge of this clock pulse. The clock pulse, which was input when the enable bit ($\overline{EL}$ / $\overline{ER}$) is in not active condition, is invalid. 2). In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock. Hence, this clock pin is not used (Open or connect this pin to VDD).	Controller
M	Input	AC signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input in to this pin.	Controller
CL1	Input	Data latch clock	1). In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block. 2). In common driver application mode, CL1 is used as a shifting clock of common output data.	Controller
$\overline{DISPOFF}$	Input	Display off Control	Control input pin to fix the driver output (SC1 - SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.	Controller
CS	Input	COM/SEG mode Control	When CS = "Low", SPLC086A is used as an 80-bit segment driver. When CS = "High", SPLC086A is set to an 80-bit common driver.	VDD/VSS
AMS	Input	Application mode select	According to the input value of the AMS and the CS pin, application mode of SPLC086A differs as shown below.	VDD/VSS

CS	AMS	Application mode	COM/SEG
0	0	4-bit parallel interface mode	SEG
0	1	1-bit serial interface mode	
1	0	Signal-type application mode	COM
1	1	Dual-type application mode	

Mnemonic	Input/ Output	Name	Function	Interface
D1_SID D2_DL D3_DM D4_DR	I/O	Display data input/serial input data/left, right data input output	1). In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode: AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode: AMS = "High"). 2). In common driver application mode, the data is shifted from D2_DL (D4_DR) to D4_DR (D2_DL), when in single type interface mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR (D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to ***4.4 Data Shift Direction According to Control Signals*** and ***4.4.3 Usage of Data PINs***)	Controller
SHL	Input	Shift direction control	When SHL = "Low", data is shifted from left to right. When SHL = "High", the direction is reversed. (refer to ***4.4 Data Shift Direction According to Control Signals***)	VDD/VSS
$\overline{EL}$ $\overline{ER}$	I/O	Enable data Input/output	1). In segment driver application mode, the internal operation is enabled only when enable input ($\overline{EL}$ or $\overline{ER}$) is "Low" (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below. 2). In common driver application mode, power down function is not used. Open these pins.	

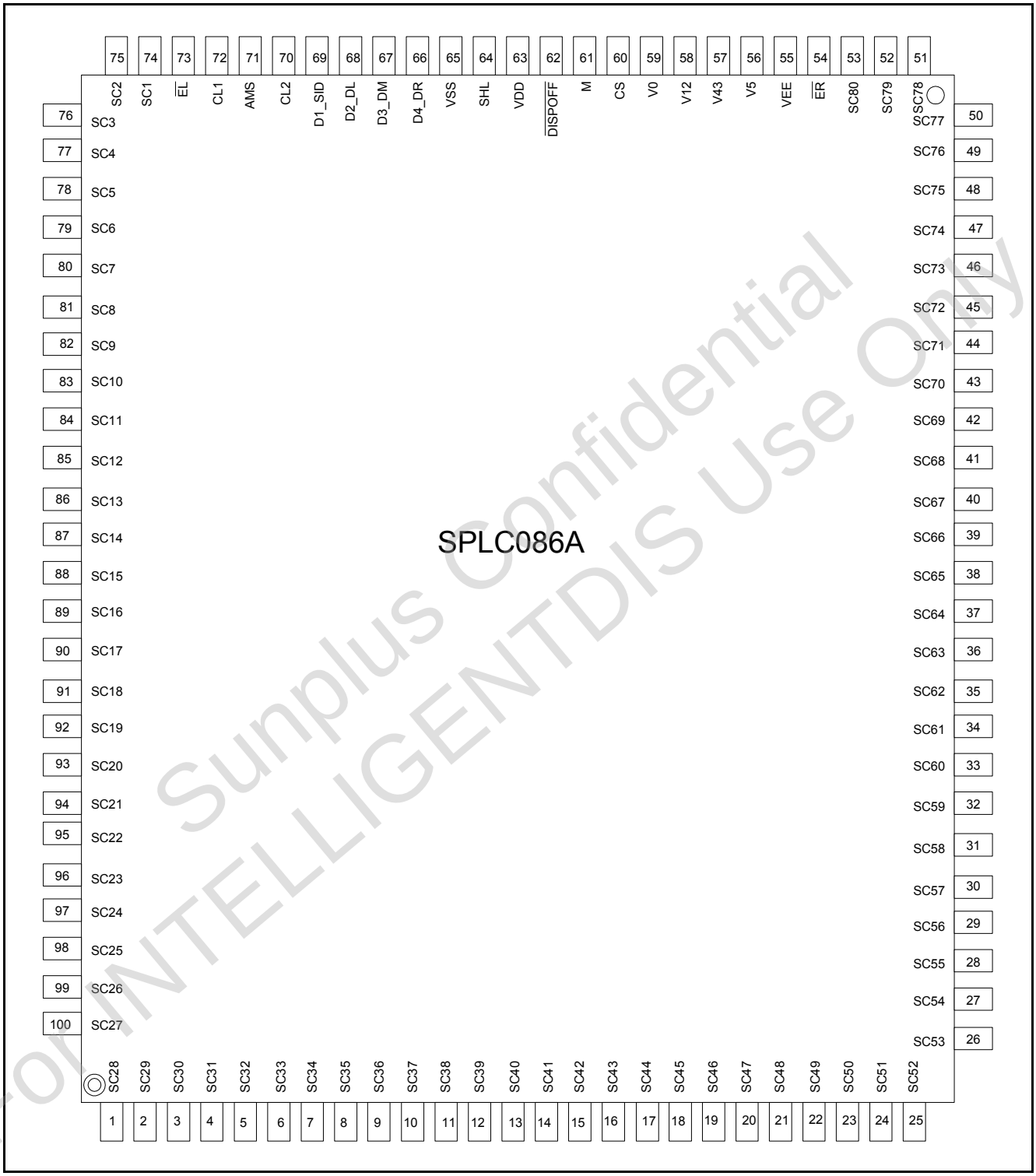
SHL	Application mode	
	$\overline{EL}$	$\overline{ER}$
L	Output (open)	Input (VSS)
H	Input (VSS)	Output (open)

4.1. Output Level Control

M	Latched data	$\overline{DISPOFF}$	Output level (SC1 - SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

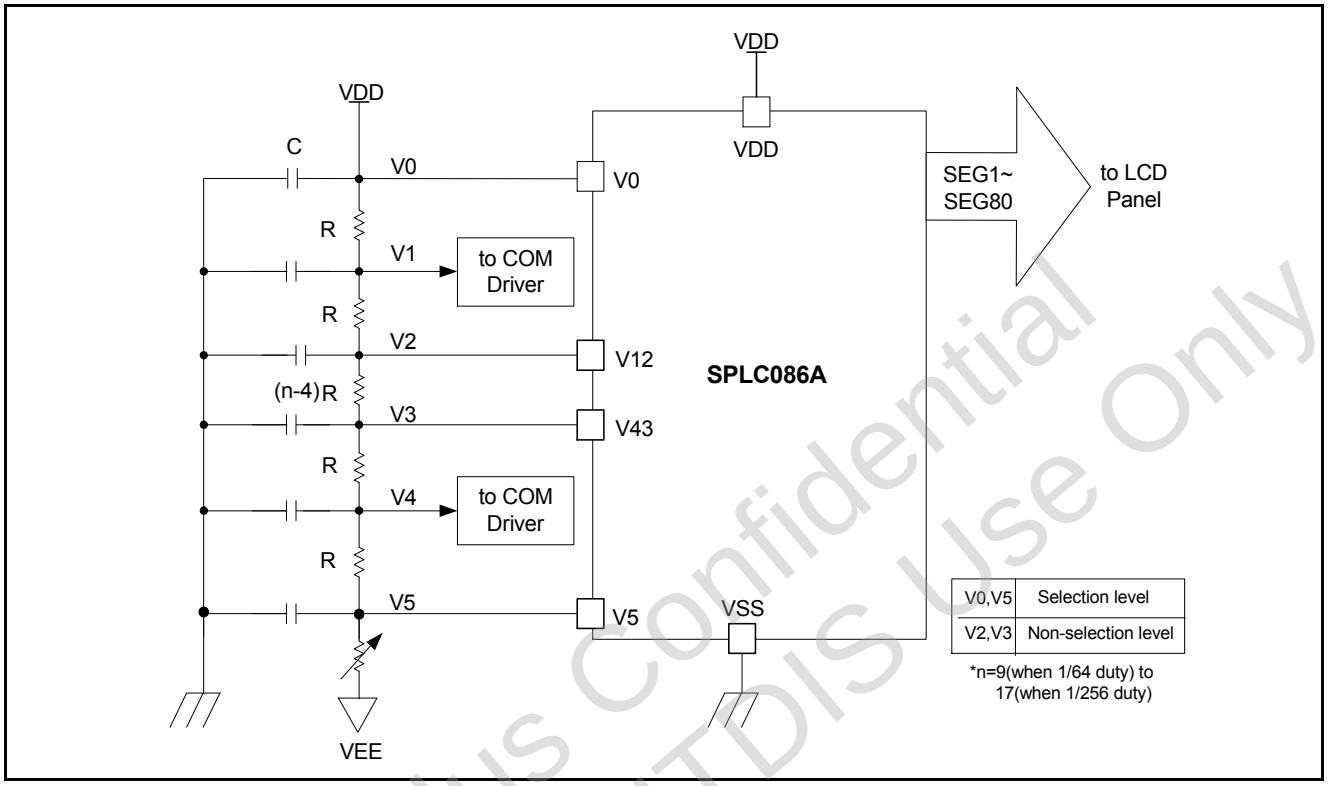
"X": don't care

4.2. SPLC086A LQFP Type (SPLC086A): 100LQFP

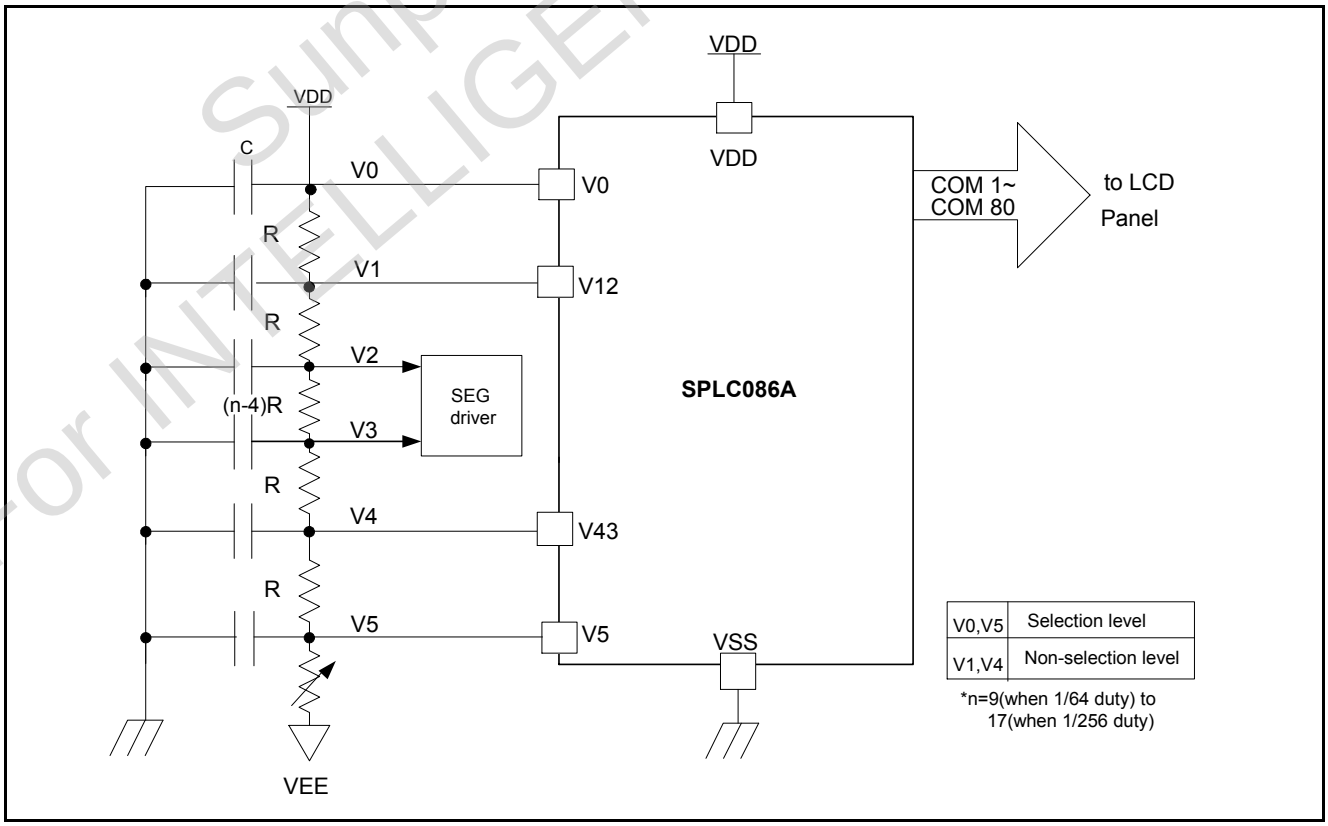


4.3. LCD Driving Voltage Application Circuits

4.3.1. Segment driver application (CS = “Low”)

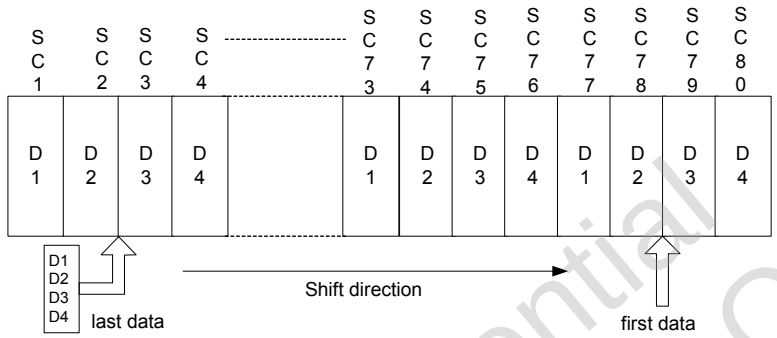
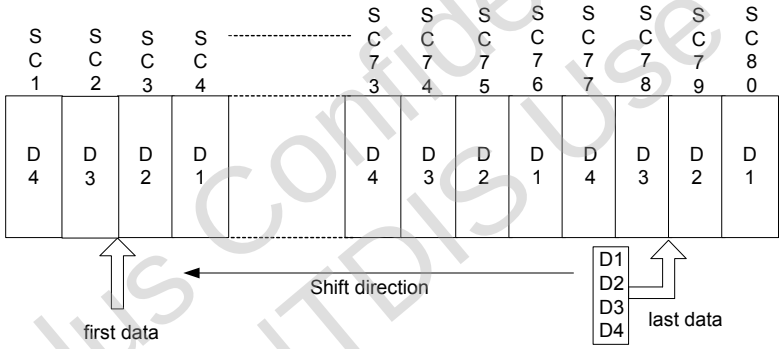
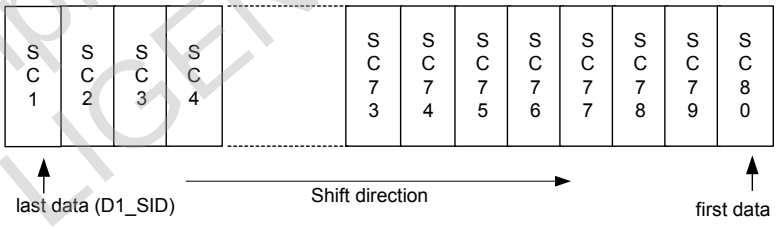
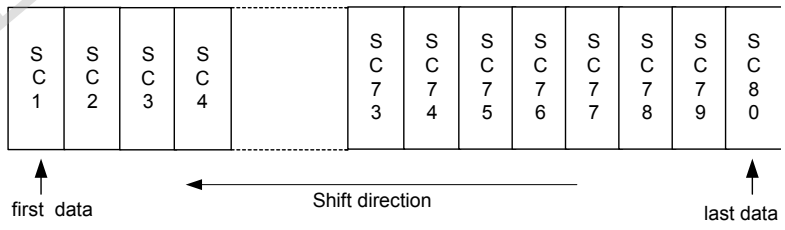


4.3.2. Common driver application (CS = “High”)

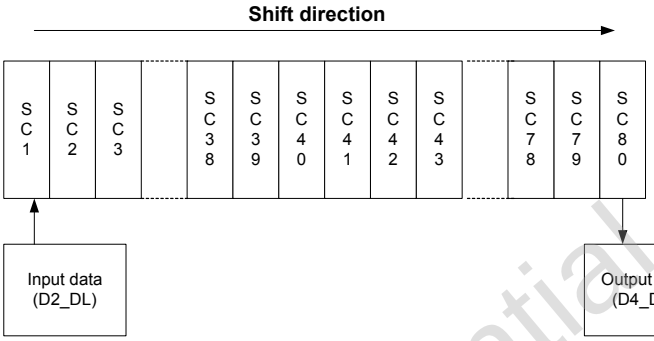
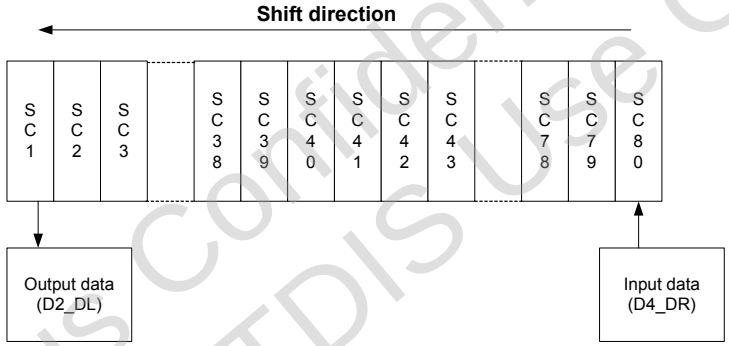
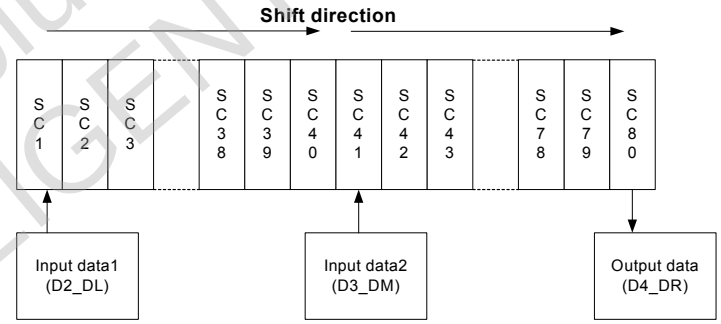
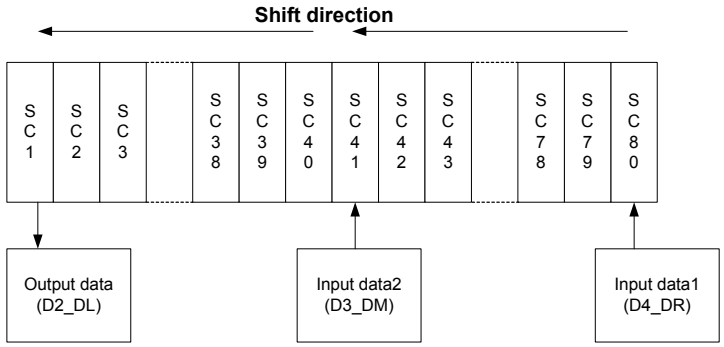


4.4. Data Shift Direction According to Control Signals

4.4.1. When CS = “Low” (segment driver application)

AMS	SHL	Application Mode	Data Direction	Input PIN
L	L	4-Bit Parallel Data Transfer Mode (SEG)		D1_SID, D2_DL, D3_DM, D4_DR,
	H			
H	L	1-Bit Serial Data Transfer Mode (SEG)		D1_SID
	H			

4.4.2. When CS = “High” (common driver application)

AMS	SHL	Application Mode	Data Direction	Input PIN
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL D3_DM
	H			D4_DR D3_DM

4.4.3. Usage of Data PINs

X = don't care

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS ="Low")	4-bit parallel interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "High")	X	SID (input)	Connect to VDD		
COM (CS = "High")	Single-type application mode (AMS = "Low")	L	Open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	Dual-type application mode (AMS = "High")	L	Open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

5. ELECTRICAL SPECIFICATIONS

5.1. Maximum Absolute Limit

Characteristic	Symbol	Value	Unit
Power supply voltage	VDD	-0.3 – +7.0	V
Driver supply voltage	V_{LCD}	0 – +30	
Input voltage	V_{IN}	-0.3 – VDD + 0.3	
Operating temperature	T_{OPR}	-30 – +85	°C
Storage temperature	T_{STG}	-55 – +150	

Note: Voltage greater than above may do damage to the circuit.

5.2. DC Characteristics

5.2.1. Segment driver application

(VSS = 0V, T_A = - 30°C - +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage1	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6.0	-	28	
Input voltage (1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	µA
Input leakage current 2 (3)	I_{IL2}	V_{IN} = VDD to VEE		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100µA		-	2.0	4.0	KΩ
Supply current (5)	I_{STBY}	f_{CL1} = 32KHz M = VSS	VSS pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32KHz f_M = 80Hz	VDD = 5.0V	-	-	5.0	mA
	I_{EE}		VDD = 3.0V	-	-	2.0	
			VDD = 5.0V	-	-	500	µA

Note1: Applied to CL1, CL2, $\overline{EL}$, $\overline{ER}$, D1_SID~D4_DR, SHL, $\overline{DISPOFF}$, M, CS, AMS pin

Note2: $\overline{EL}$, $\overline{ER}$ pin

Note3: V0, V12, V43, V5 pin

Note4: V_{LCD} = VDD - VEE, V0 = VDD = 5.0V, V5= VEE = -23V
V12 = VDD-2/n (V_{LCD}), V43 = VEE+2/n (V_{LCD}), n = 17 (1/256 duty, 1/17 bias)

Note5: V0 = VDD, V12 = 1.71V (VDD = 5.0V) or - 0.06V (VDD = 3.0V),
V43 = -19.71V (VDD = 5.0V) or -19.94V (VDD = 3.0V), V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias) 4-bit parallel interface mode
I_{STBY}: VDD = 5.0V, f_{CL2} = 5.12MHz, SHL = VSS, $\overline{DISPOFF}$ = VDD, M = VSS, display data pattern = 0000
I_{DD} : VDD = 3.0V, f_{CL2} = 4.0MHz, display data pattern = 0101
VDD = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101
I_{EE}: VDD = 5.0V, f_{CL2} = 5.12MHz, display data pattern = 0101, VEE pin

5.2.2. Common driver application

(VSS = 0V, T_A = - 30°C – +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage	VDD	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = VDD - VEE		6.0	-	28	
Input voltage (1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		VDD-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = VDD to VSS		-10	-	10	μA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, VDD = 5.0V (PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN} = VDD to VEE		-25	-	25	
On resistance (5)	R_{ON}	I_{ON} = 100μA		-	2.0	4.0	KΩ
Supply current (6)	I_{STBY}	f_{CL1} = 32KHz	VSS pin	-	-	100	μA
	I_{DD}	f_{CL1} = 32KHz, f_M = 80Hz	VDD = 5.0V	-	-	200	
			VDD = 3.0V	-	-	120	
	I_{EE}		VDD = 5.0V	-	-	150	

Note1: Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFF , M, CS, AMS pin

Note2: Pull-up input pins: CL2, D1_SID, D3_DM (AMS = HIGH), EL (SHL = LOW), ER (SHL = HIGH)

Note3: D2_DL (SHL = HIGH), D4_DR (SHL = LOW) pin

Note4: V0, V12, V43, V5 pin

Note5: V_{LCD} = VDD-VEE, V0 = VDD = 5.0V, V5 = VEE = -23V
V12 = VDD-1/n(V_{LCD}), V43 = VEE+1/n(V_{LCD}), n = 17(1/256 duty, 1/17 bias)

Note6: V0 = VDD, V12 = 3.35V (VDD = 5.0V) or 1.47V (VDD = 3.0V),
V43 = -21.35V (VDD = 5.0V) or -21.47V (VDD = 3.0V), V5 = VEE = -23V, no-load condition (1/256 duty, 1/17 bias) single-type mode operation: AMS = VSS, SHL = VSS, DISPOFF = VDD
D1_SID = D3_DM = VDD, D4_DR = OPEN, EL = ER = OPEN,
I_{STBY}: VDD = 5.0V, M = VSS, D2_DL = VSS
I_{DD}: f_M = 80Hz, D2_DL = VDD
VDD = 3.0V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
VDD = 5.0V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
I_{EE}: f_M = 80Hz, D2_DL = VDD
VDD = 5.0V, current through VEE Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...

5.3. AC Characteristics

5.3.1. Segment driver application

(VSS = 0V, T_A = - 30°C – +85°C)

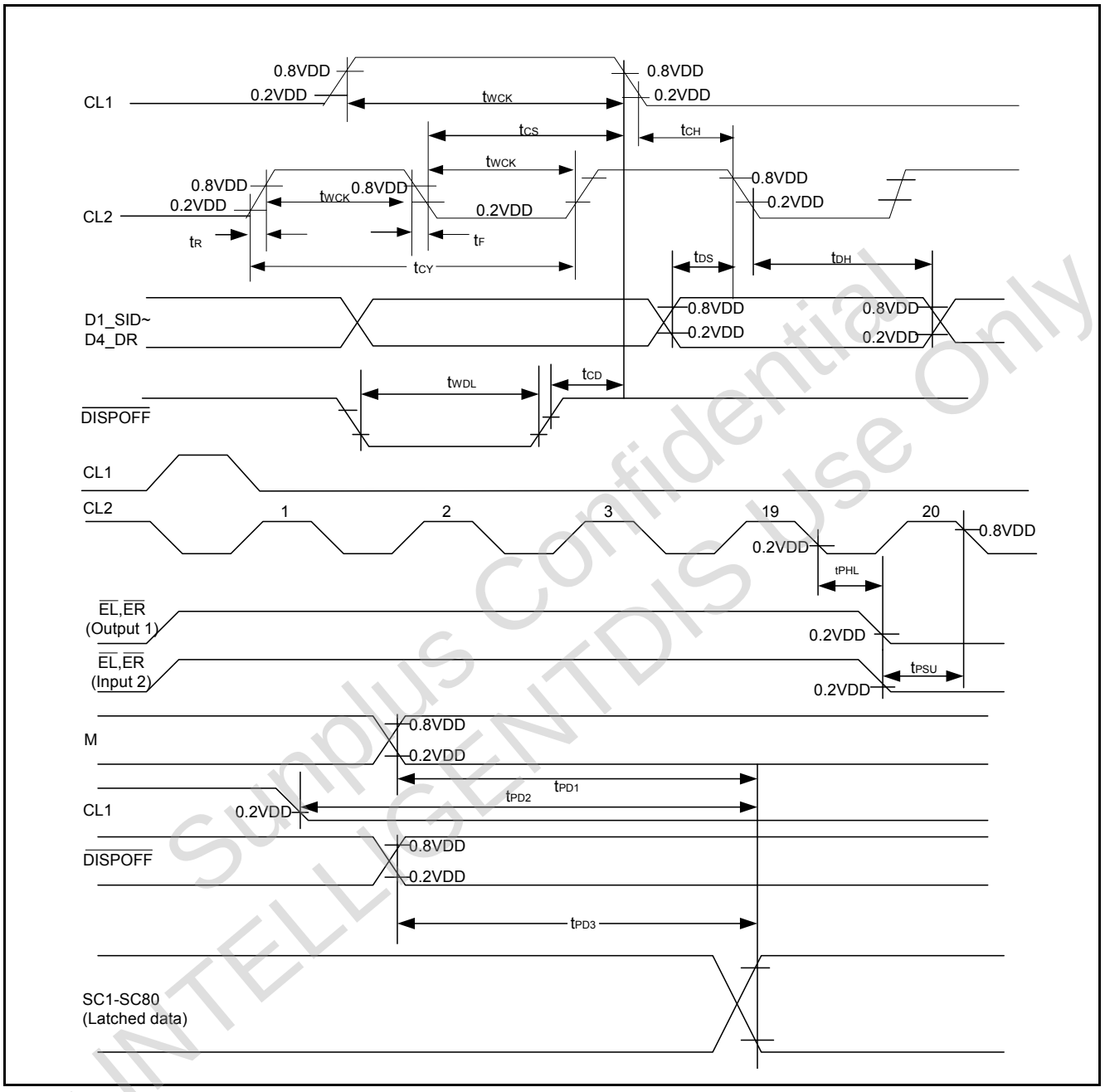
Characteristic	Symbol	Test Condition	(1) VDD = 5.0V ±10%			(2) VDD = 3.0V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	$\overline{EL}$ Output	-	-	60	-	-	125	
		$\overline{ER}$ Output			60			125	
$\overline{EL}$, $\overline{ER}$ set-up time	t_{PSU}	$\overline{EL}$ Input	30	-	-	65	-	-	
		$\overline{ER}$ Input	30			65			
$\overline{DISPOFF}$ low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
$\overline{DISPOFF}$ clear time	t_{CD}	-	100	-	-	100	-	-	ns
M – OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
$\overline{DISPOFF}$ - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

5.3.2. Common driver application

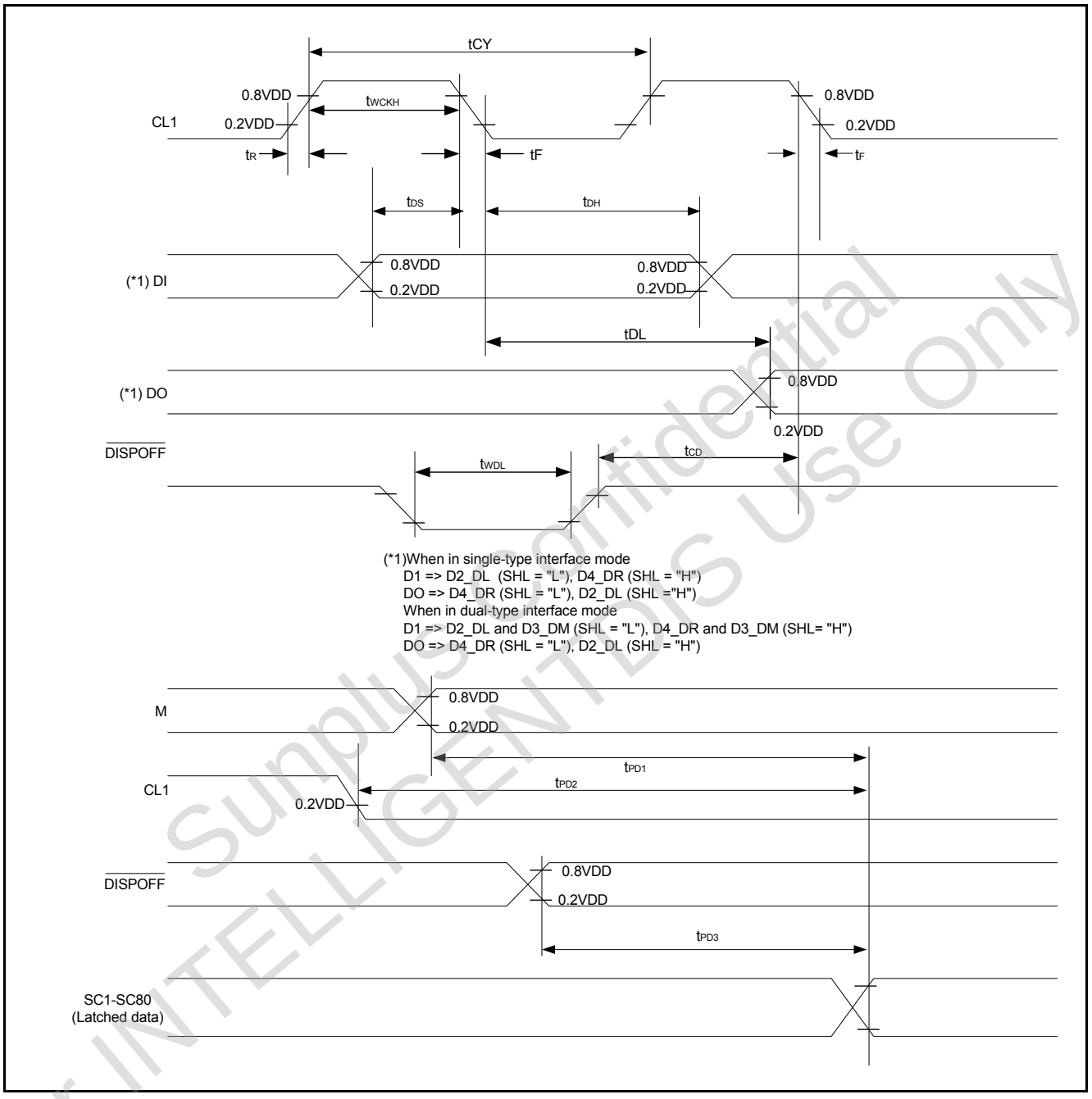
(VSS = 0V, T_A = - 30°C – +85°C)

Characteristic	Symbol	Test Condition	(1) VDD = 5.0V ±10%			(2) VDD = 3.0V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
$\overline{DISPOFF}$ low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
$\overline{DISPOFF}$ clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	
M - OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
$\overline{DISPOFF}$ - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

5.3.3. Segment driver application timing



5.3.4. Common driver application timing

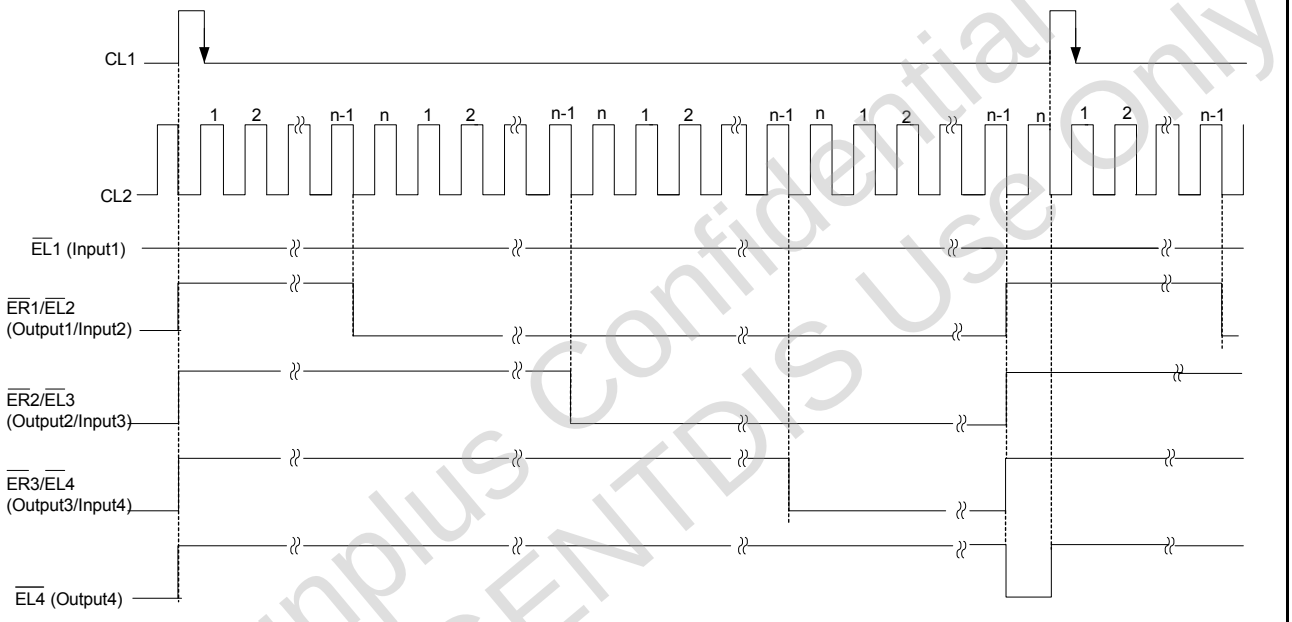


5.4. Power Down Function

In the case of cascade connection of segment mode drivers, power consumption.
SPLC086A has a "power down function" in order to reduce the

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	$\overline{ER}$	$\overline{EL}$	While $\overline{ER}$ ="Low", current driver is enabled.	Disabled
H	$\overline{EL}$	$\overline{ER}$	While $\overline{EL}$ ="Low", current driver is enabled.	Disabled

Note: In the case of common driver application, power down function does not work.

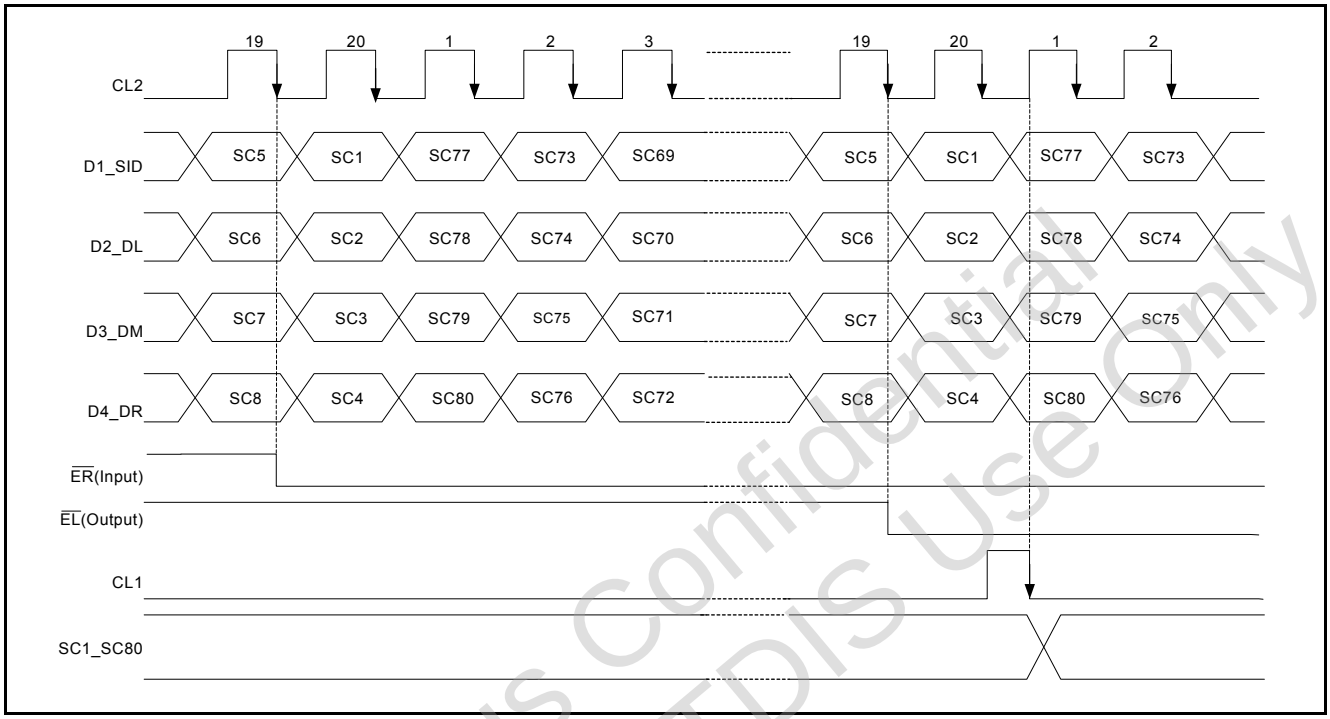


Note1: SHL = "High" ($\overline{EL}$ = Input, $\overline{ER}$ = Output)
Current SPLC086A's $\overline{ER}$ must be connected to the next SPLC086A's $\overline{EL}$.
Note2: When in 4-bit parallel interface mode: n = 20
When in 1-bit serial interface mode: n = 80

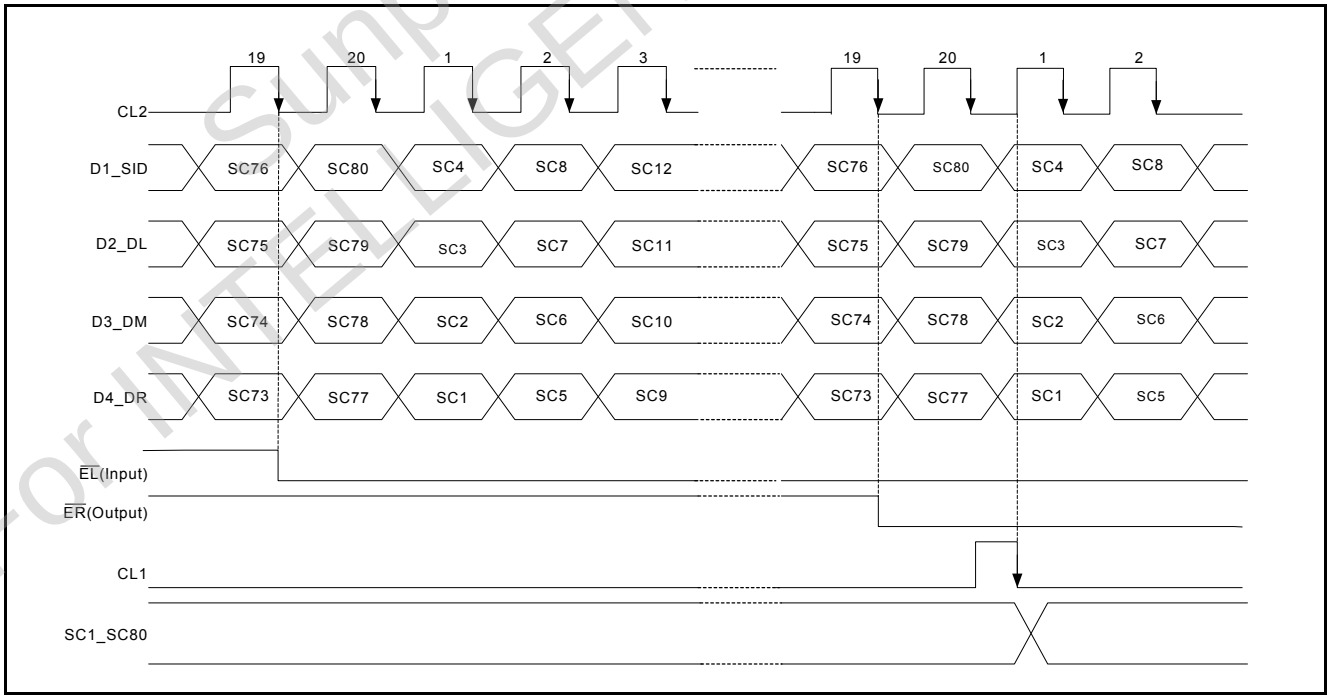
5.5. Operation Timing Diagram

5.5.1. 4-bit parallel mode interface segment driver

1.) When SHL = "Low"

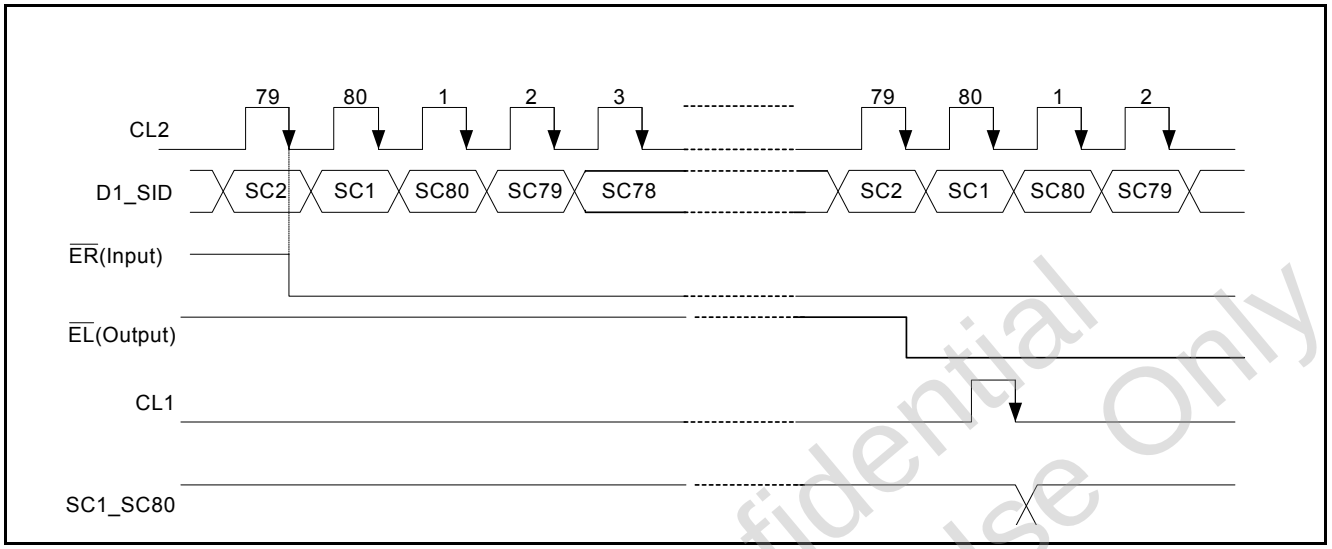


2.) When SHL = "High"

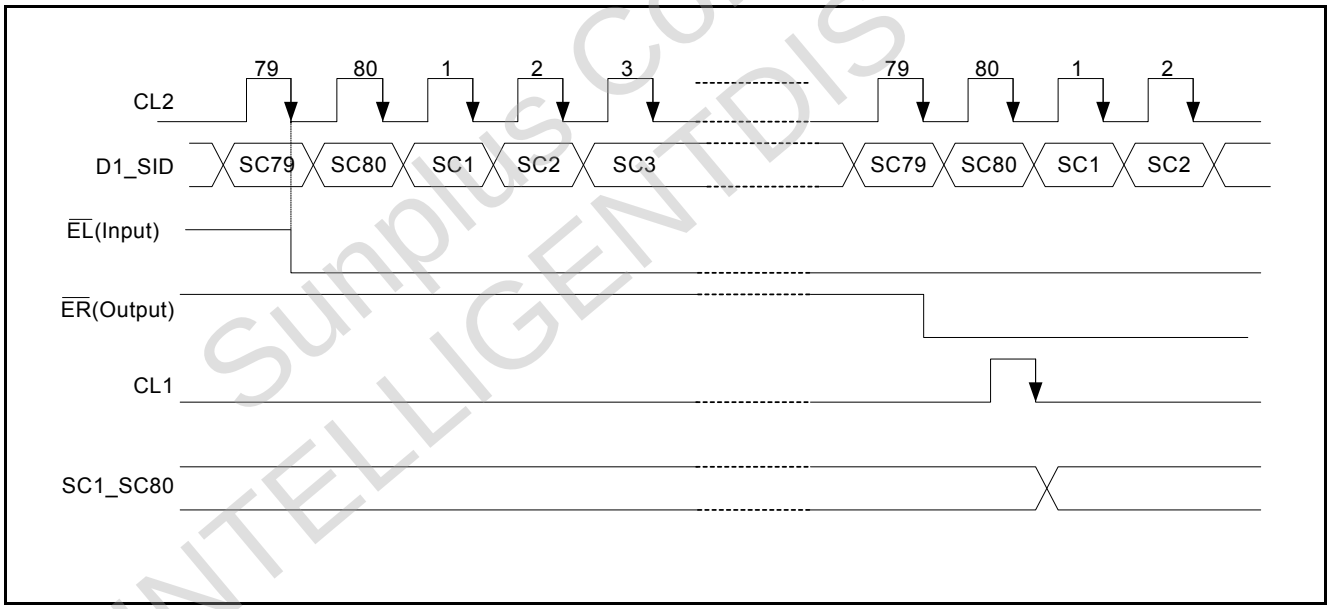


5.5.2. 1-bit serial mode interface segment driver

1.) When SHL = “Low”

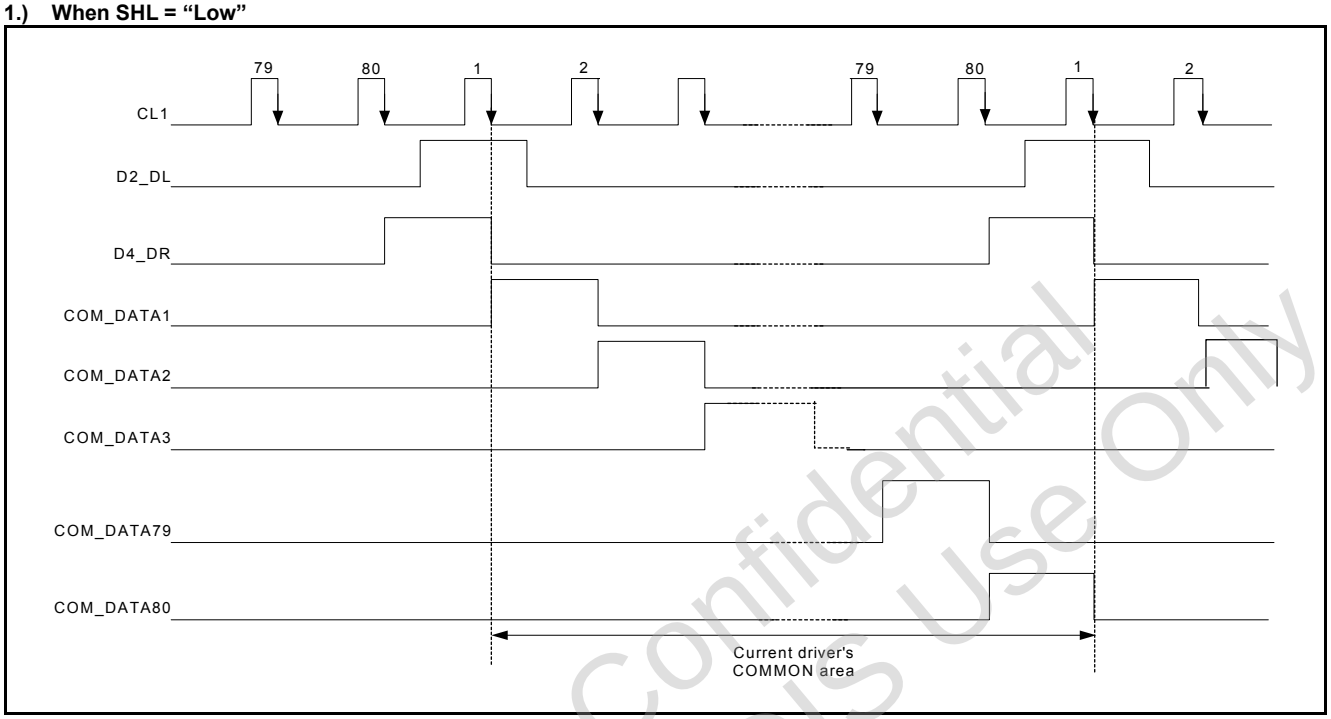


2.) When SHL = “High”

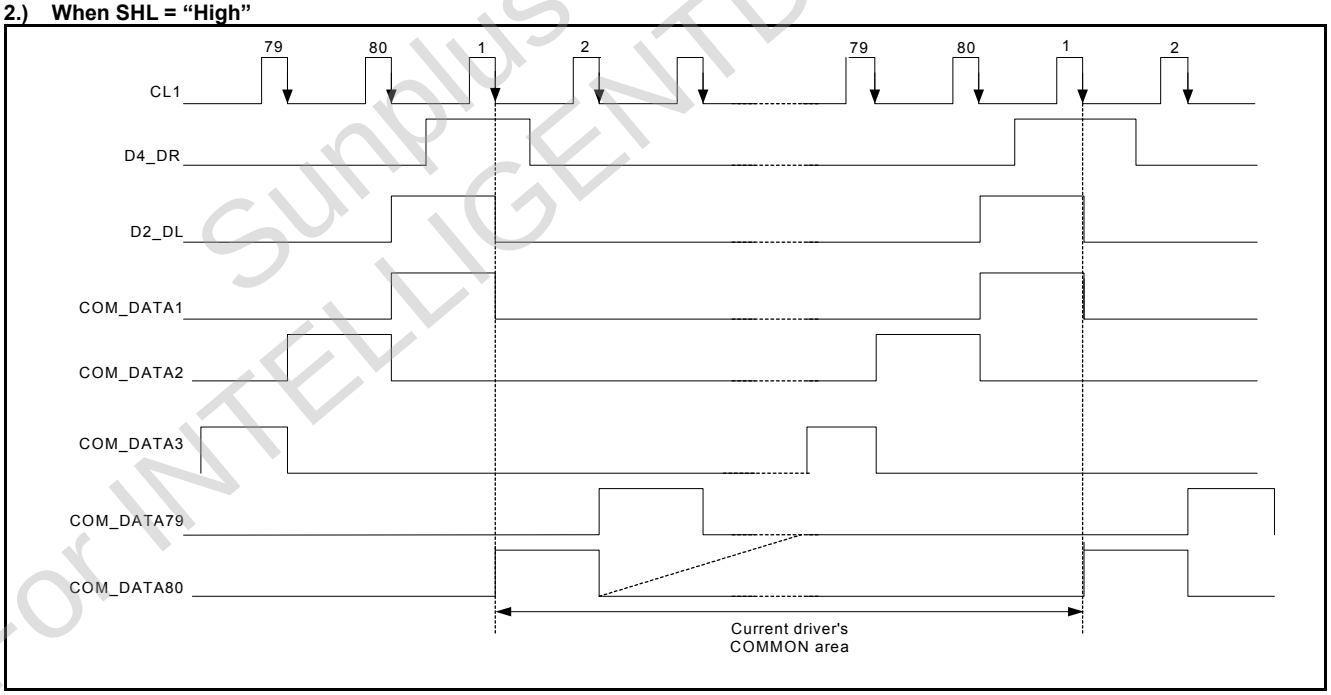


5.5.3. Single-type interface mode common driver

1.) When SHL = “Low”

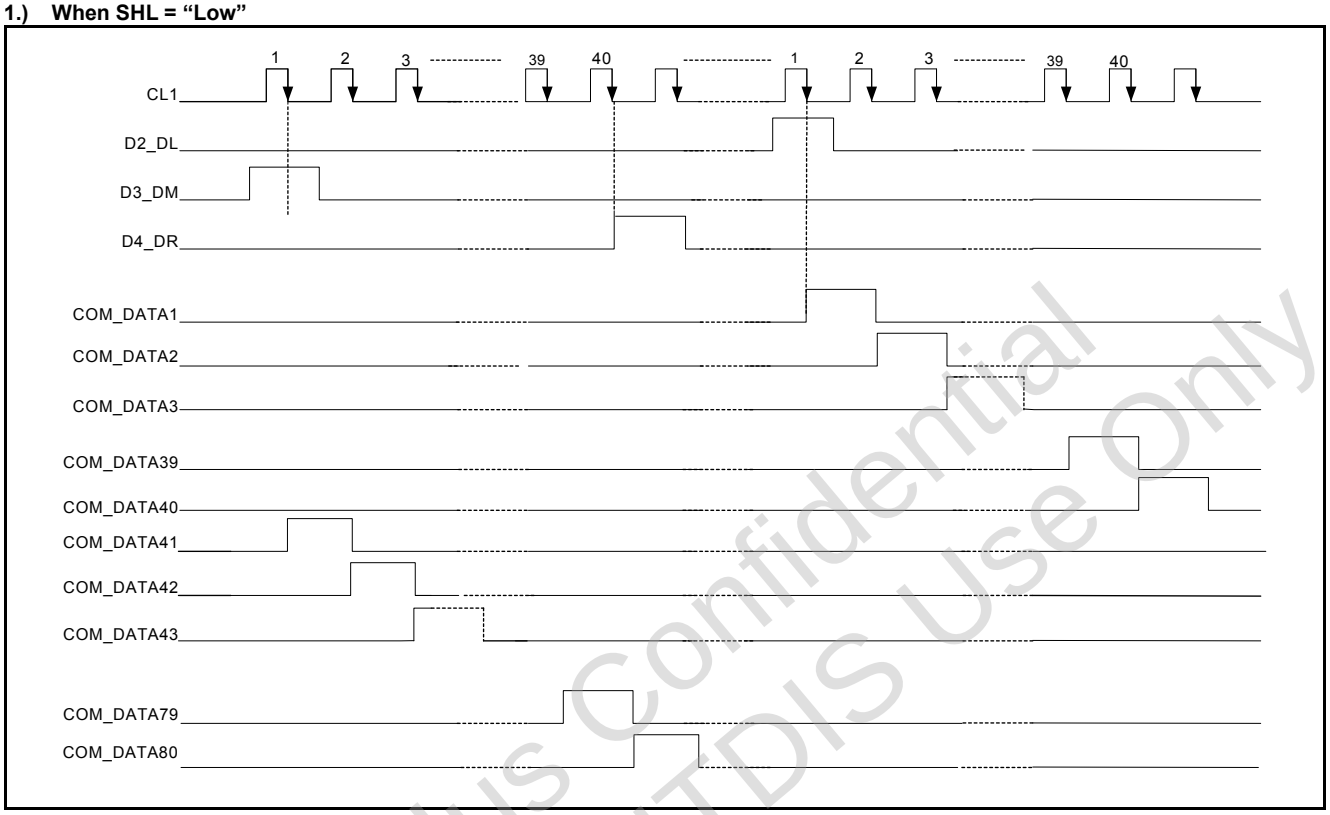


2.) When SHL = “High”

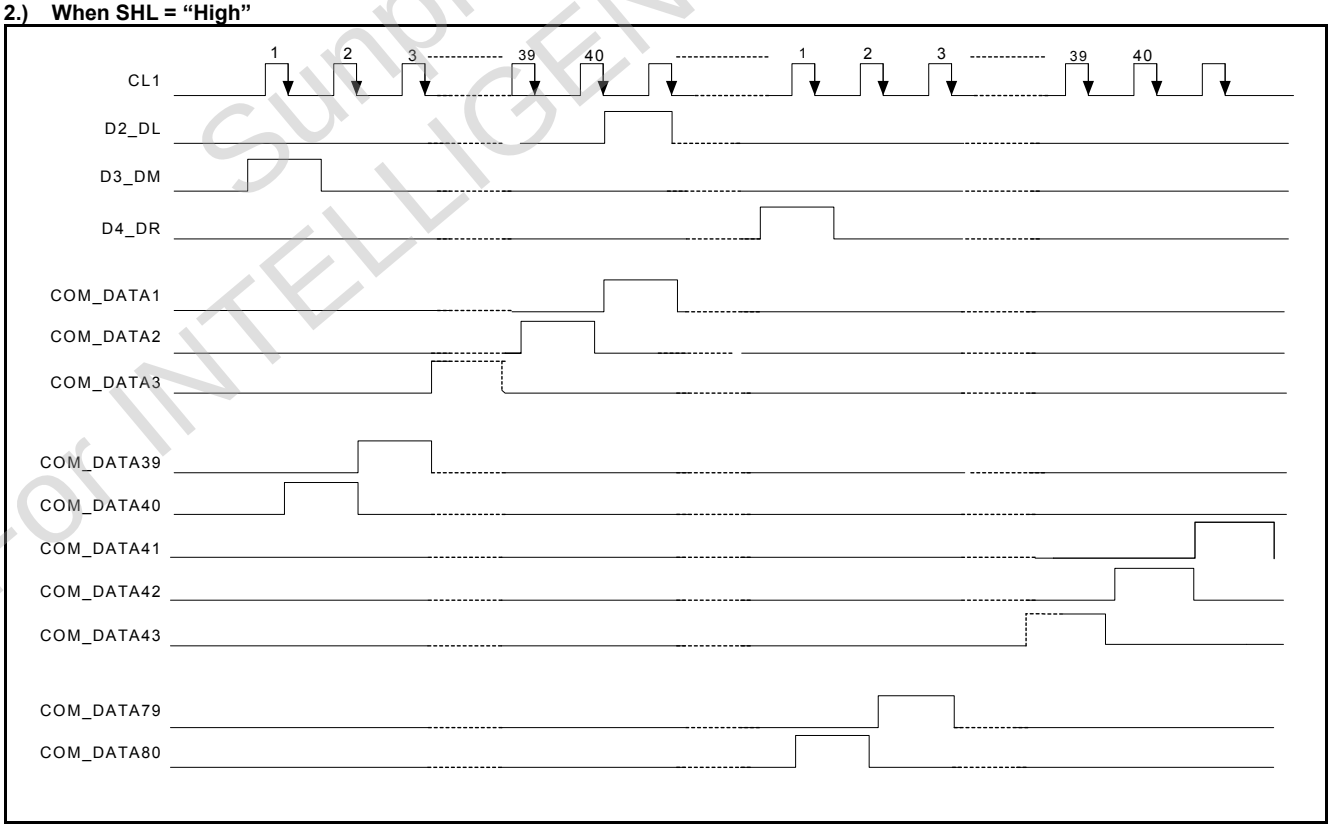


5.5.4. Dual-type interface mode common driver

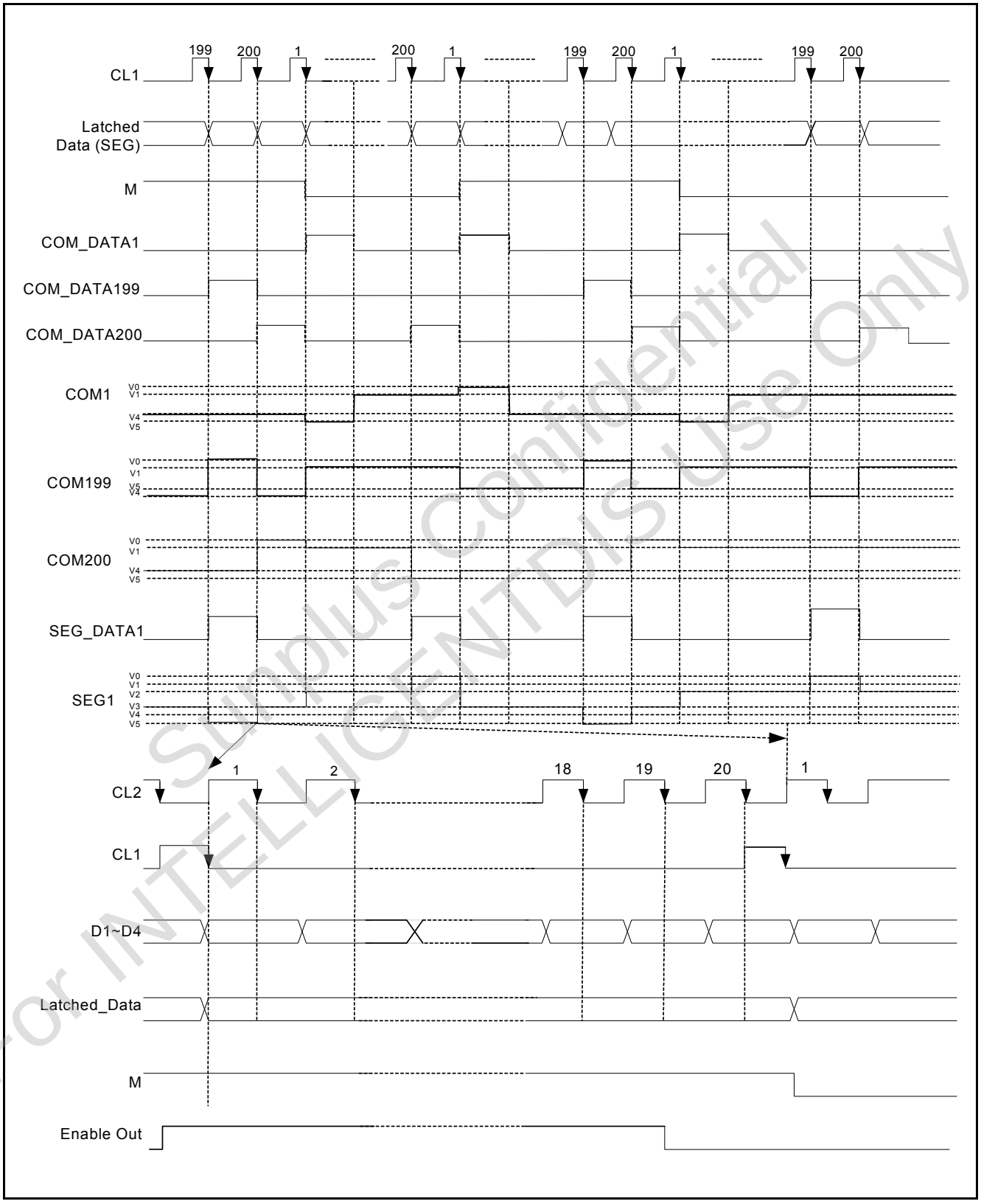
1.) When SHL = "Low"



2.) When SHL = "High"



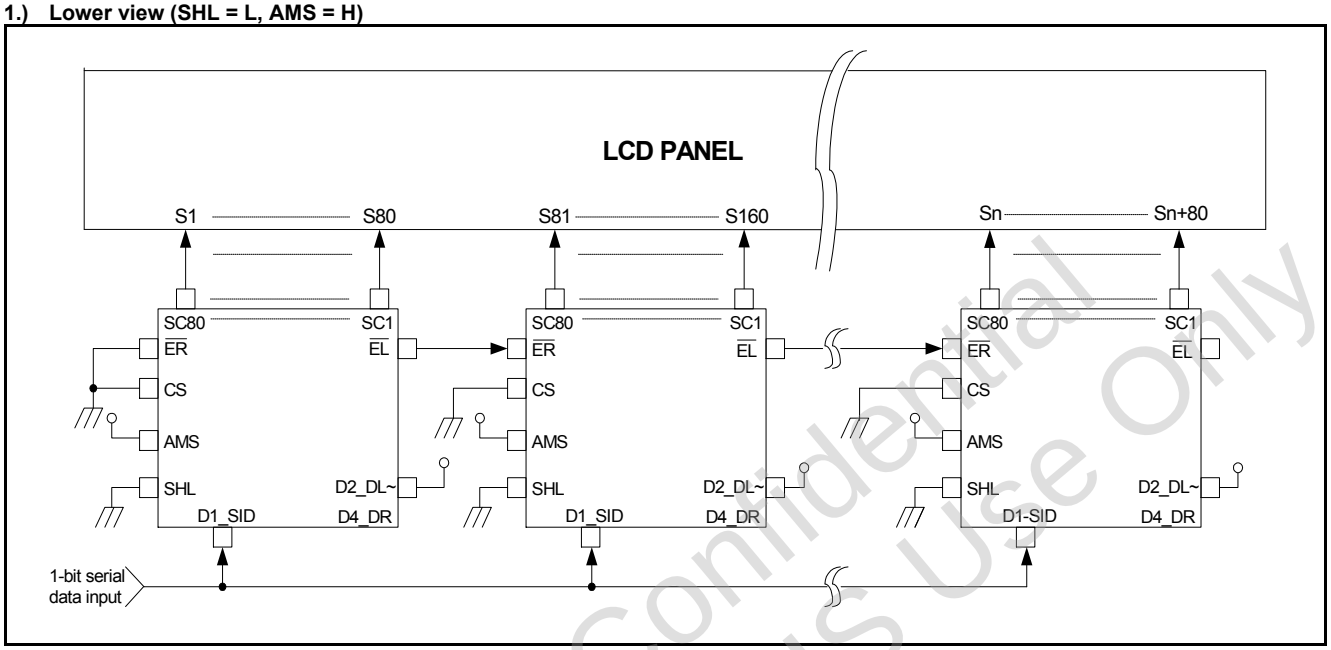
5.5.5. Common/segment driver timing (1/200 duty)



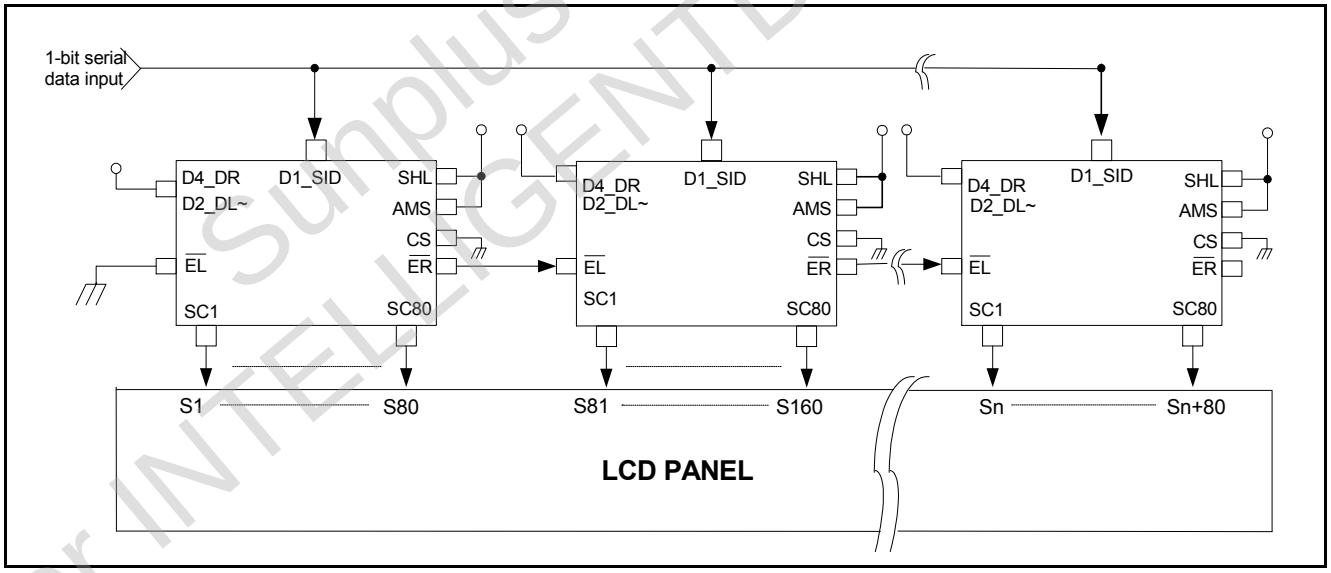
6. APPLICATION CIRCUITS

6.1. 1-Bit Serial Interface Mode (80-ch Segment Driver)

1.) Lower view (SHL = L, AMS = H)

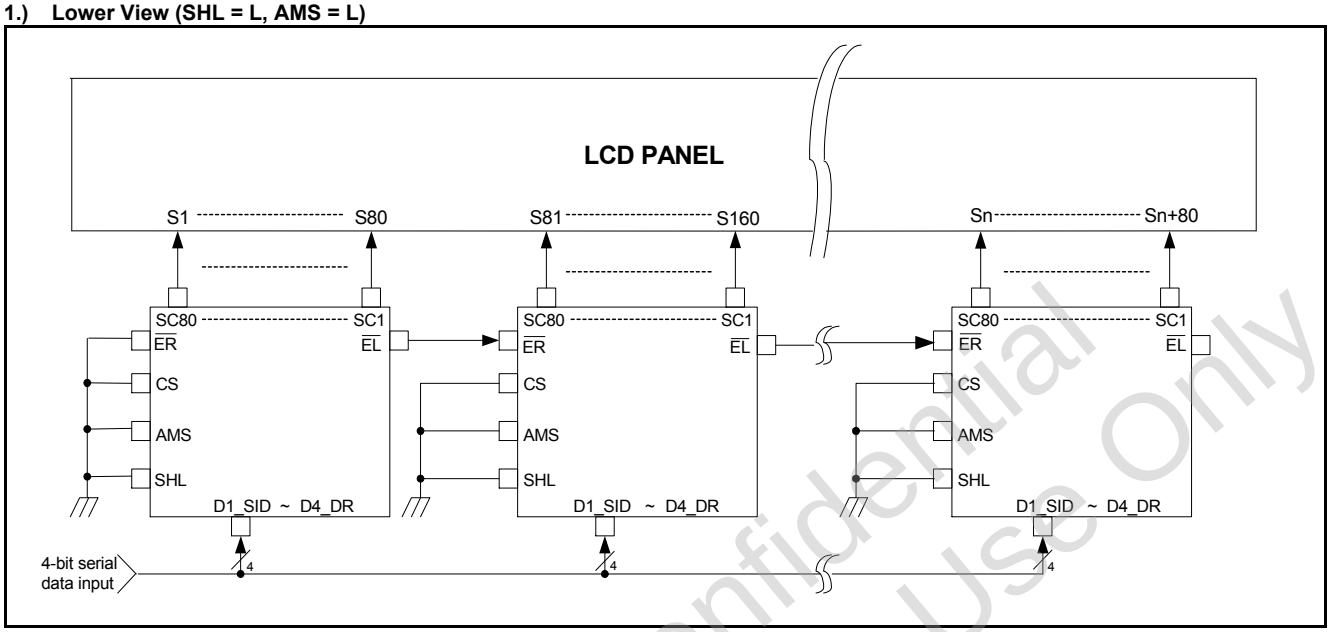


2.) Upper view (SHL = H, AMS = H)

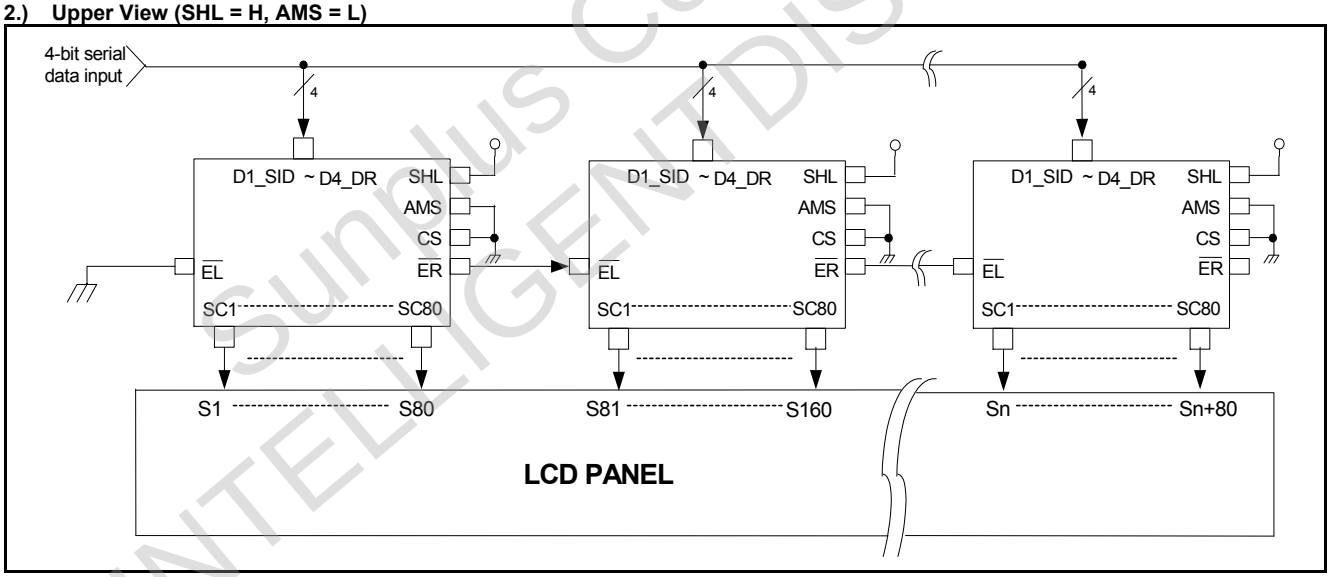


6.2. 4-Bit Parallel Interface Mode (80-ch Segment Driver)

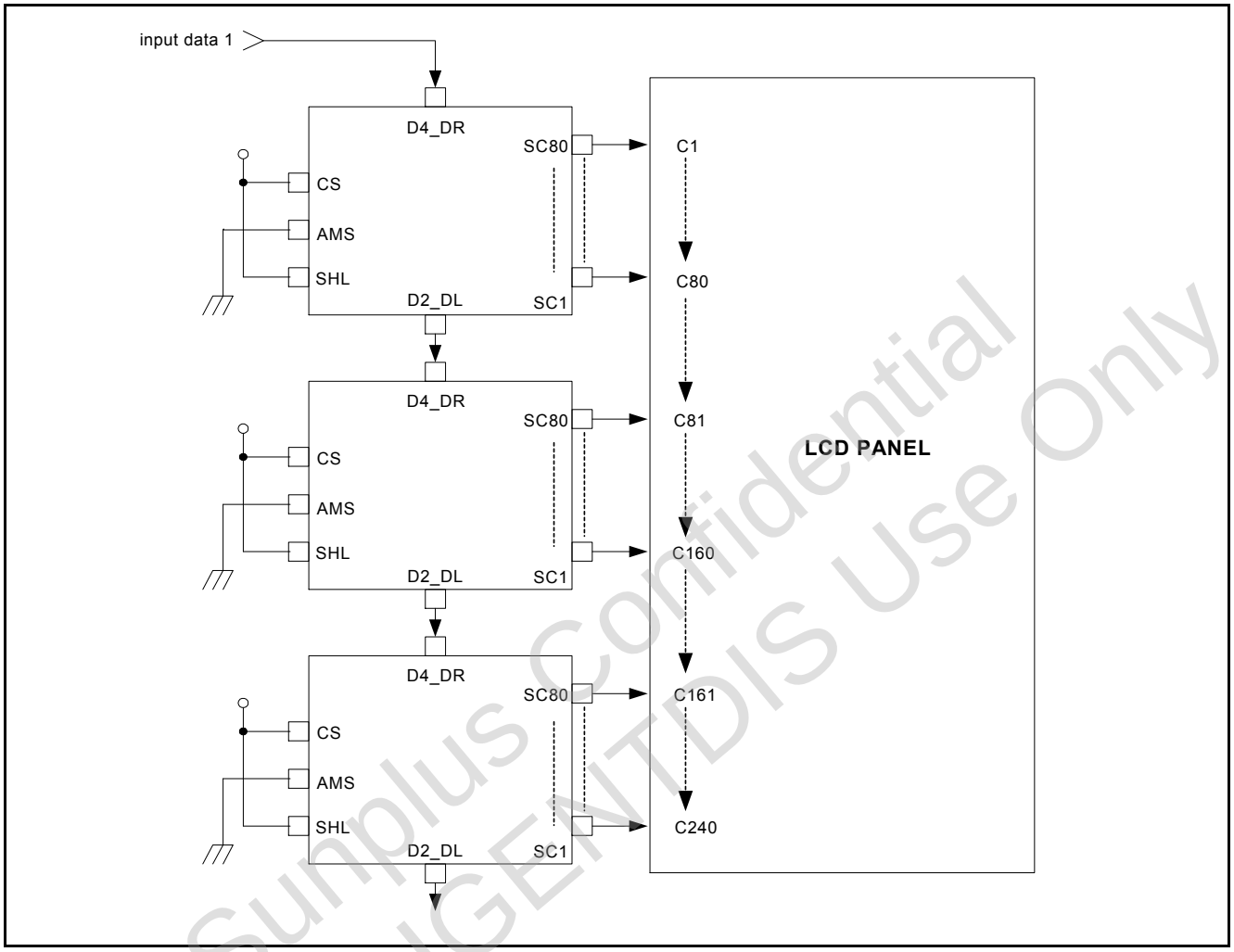
1.) Lower View (SHL = L, AMS = L)



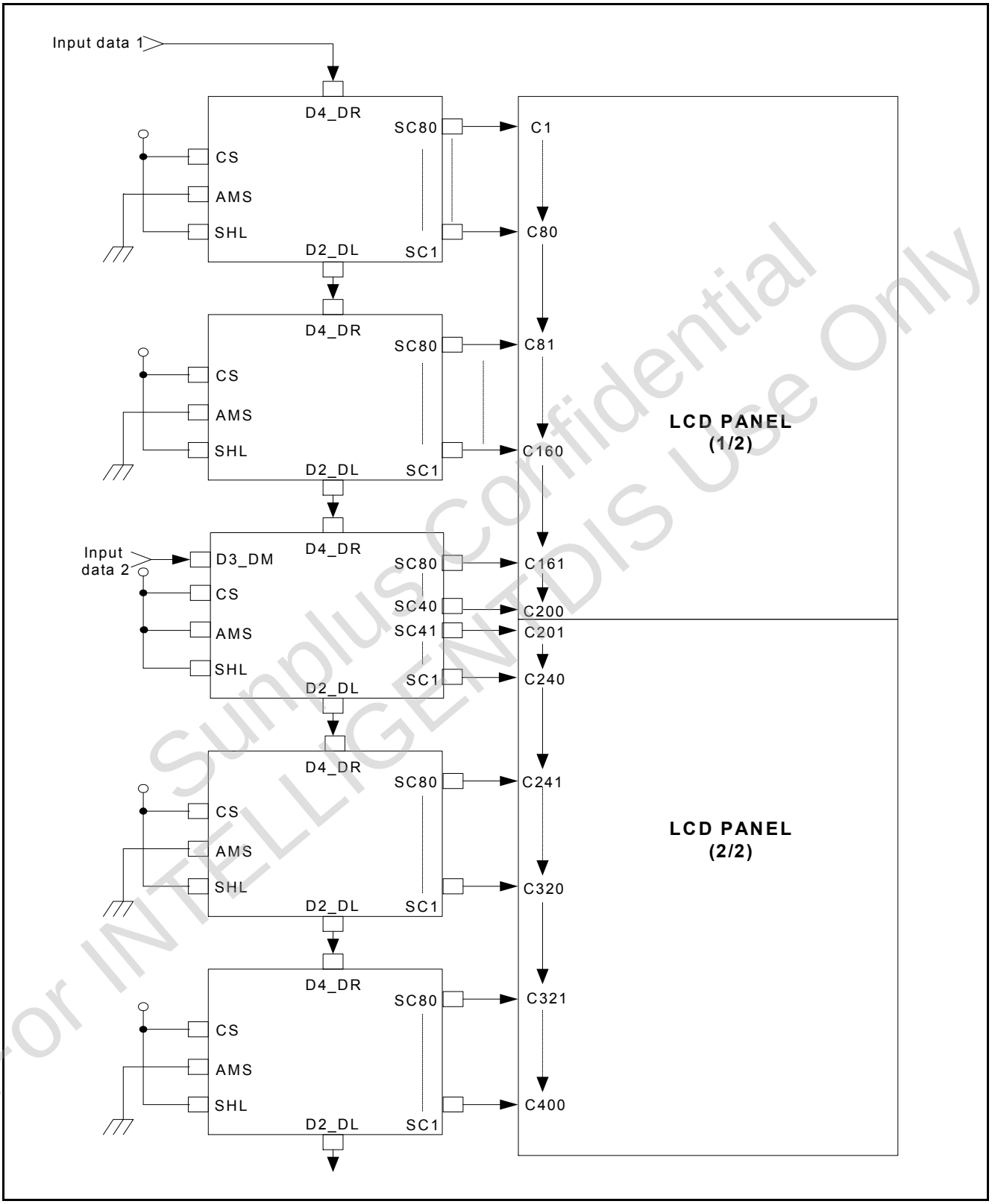
2.) Upper View (SHL = H, AMS = L)



6.3. Single-Type Interface Mode (80-ch Common Driver)

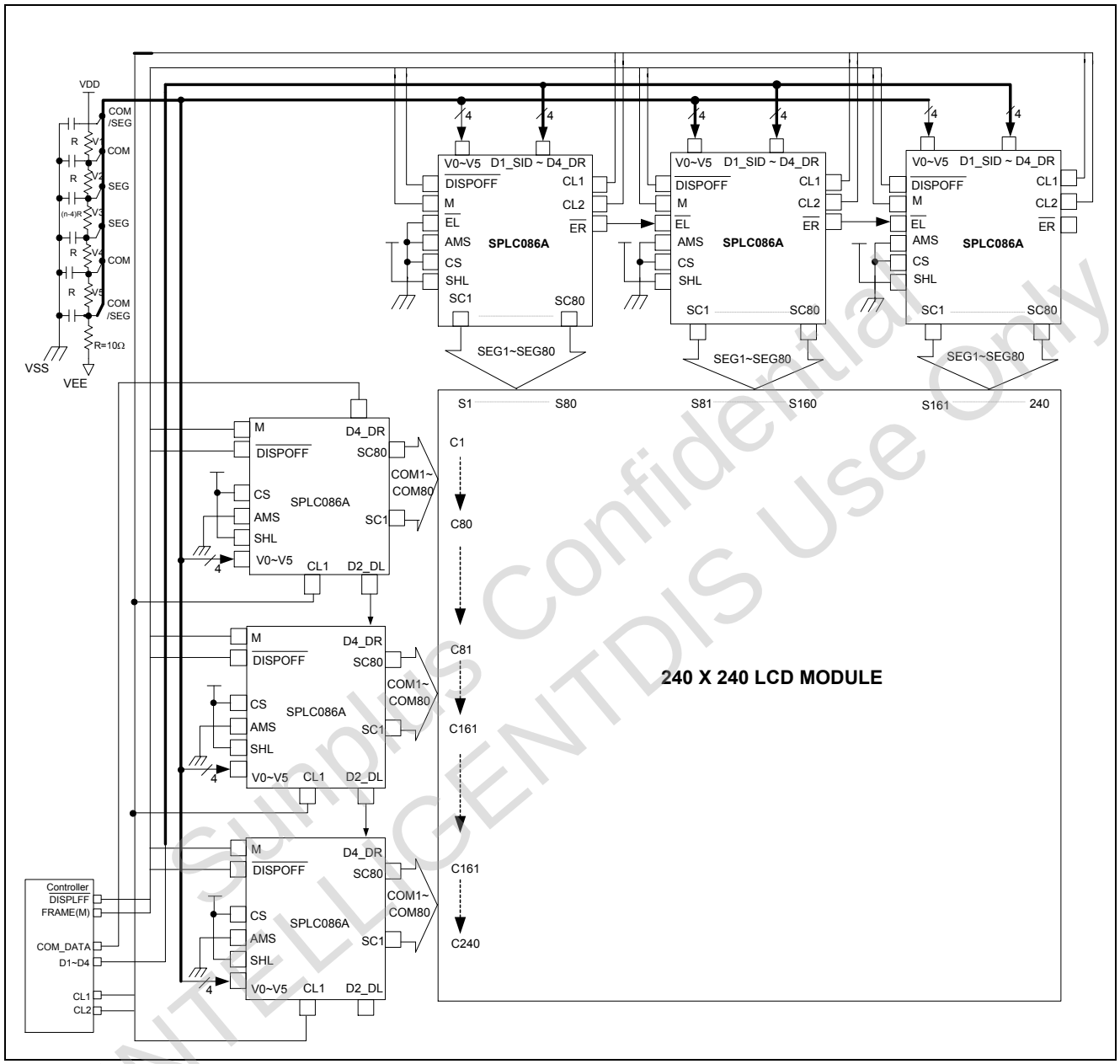


6.4. Dual-Type Interface Mode (40-ch + 40-ch Common Driver)



Note: Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In case, 1/200 duty can be used to drive the 400 common LCD panel.

6.5. Application Circuit Example



7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

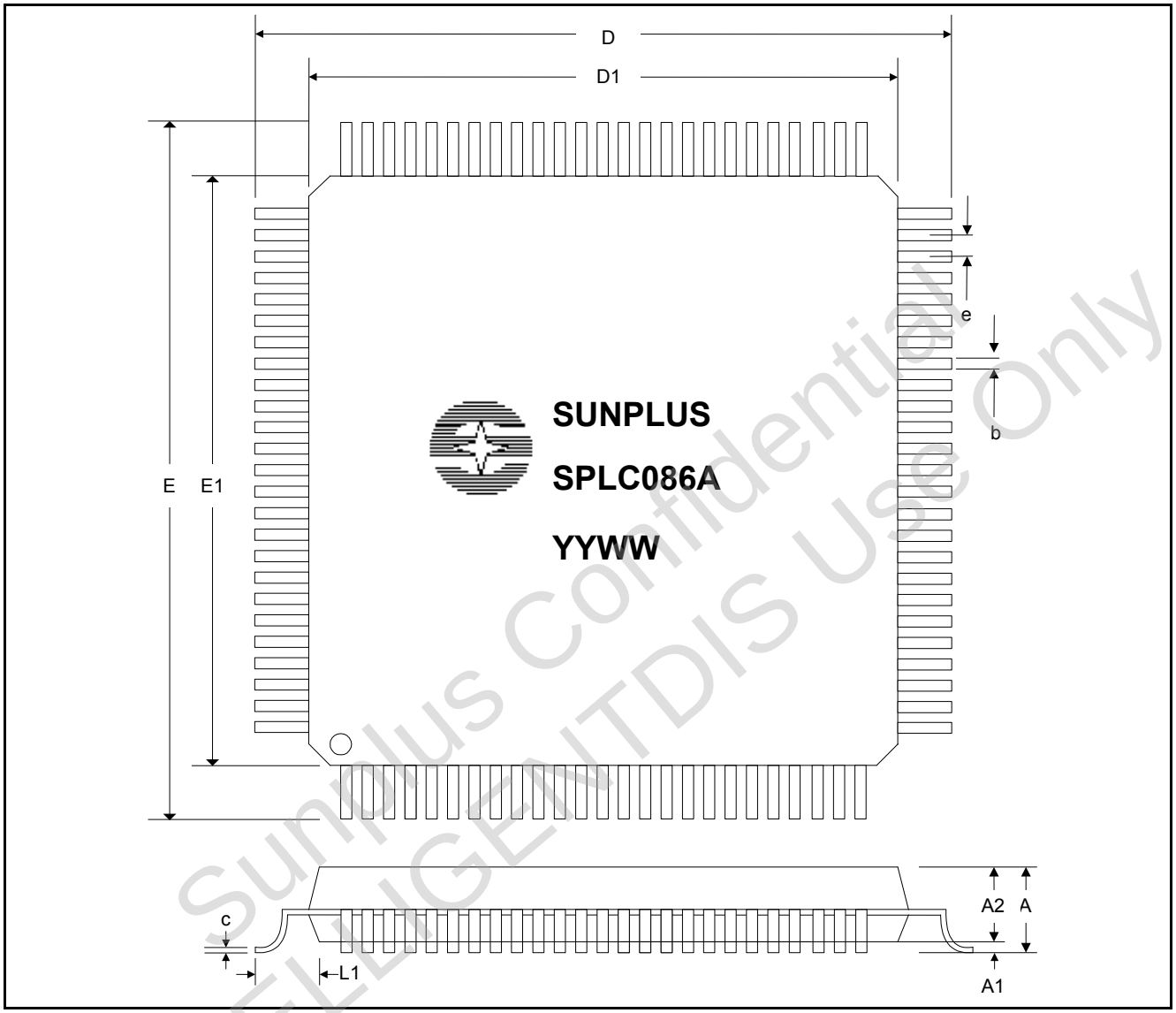
7.2. Ordering Information

Product Number	Package Type
SPLC086A-NnnV-C	Chip form
SPLC086A-NnnV-PL08	Package form - 100LQFP
SPLC086A-NnnV-FL08	Green package form - 100 LQFP

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

7.3. Package Information



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
D	15.85	16.00	16.15	Millimeter
D1	13.90	14.00	14.10	Millimeter
E	15.85	16.00	16.15	Millimeter
E1	13.90	14.00	14.10	Millimeter
L1	1.00 REF			Millimeter
b	0.17	0.22	0.27	Millimeter
c	0.09	-	0.20	Millimeter
e	0.50 BSC			Millimeter

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 03, 2004	1.0	1. Modify “4. SIGNAL DESCRIPTIONS“ add “add a resistor(10ohm) to V5 and VEE to resist power bounce." 2. Correct t_{CY} value: 250ns@5V, 500ns@3V 3. Remove Preliminary	6 15
OCT. 16, 2003	0.3	1. Modify “6.5 Application Circuit Example“ 2. Remove pad assignment and locations	
JAN. 11, 2002	0.2	1. Add Sunplus logo in the “*7.1 PAD Assignment (SPLC086A)*” 2. Redefine "Product number" in the “*7.2 Ordering Information*” 3. Correct *“7.5 Package Information*” 4. Modify DISPOFFB to $\overline{\text{DISPOFF}}$, ERB to $\overline{\text{ER}}$ and ELB to $\overline{\text{EL}}$.	27 27 30
OCT. 15, 2001	0.1	Original	