SECTION 10
ELECTRICAL CHARACTERISTICS

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of the MC68360. Refer to Section 11 Ordering Information and Mechanical Data for specific part numbers corresponding to voltage, frequency, and temperature ratings.

10.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage[1, 2]	V_{CC}	–0.3 to +6.5	V
Input Voltage[1, 2]	V_{in}	–0.3 to +6.5	V
Operating Temperature Range (CQFP and PGA for normal and extended temperature part)	T_A	0 to 70 or –40 to +85	°C
Maximum operating Junction Temperature (BGA only)	T_J	115	°C
Minimum operation Ambient Temperature (BGA only)	T_A	0	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.

The following ratings define a range of conditions in which the device will operate without being damaged. However, sections of the device may not operate normally while being exposed to the electrical extremes.

10.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance—Junction to Case 240-Pin QFP 241-Pin PGA 357-Pin BGA	θ_{JC}	2 7 8	°C/W
Thermal Resistance—Junction to Ambient 240-Pin QFP 241-Pin PGA	θ_{JA}	27.4 22.8	°C/W
Thermal Resistance—Junction to Ambient 357-pin BGA	θ_{JA}	47[1] 30[2] 20[3]	°C/W

Notes:
1. Assumes natural convection and a single layer board (no thermal vias).
2. Assumes natural convection, a multi layer board with thermal vias[4], 1.5 watt 68360 dissipation, and a board temperature rise of 30°C above ambient.
3. Assumes natural convection, a multi layer board with thermal vias[4],1.5 watt 68360 dissipation, and a board temperature rise of 15°C above ambient.
4. For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, "Plastic Ball Grid Array Application Note" available from your local Motorola sales office.

$T_J = T_A + (P_D \bullet \theta_{JA})$
$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$
where:
$P_{I/O}$ is the power dissipation on pins.

10.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

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where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts—Chip Internal Power
$P_{I/O}$= Power Dissipation on Input and Output Pins—User Determined

For most applications, $P_{I/O} < 0.3 * P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

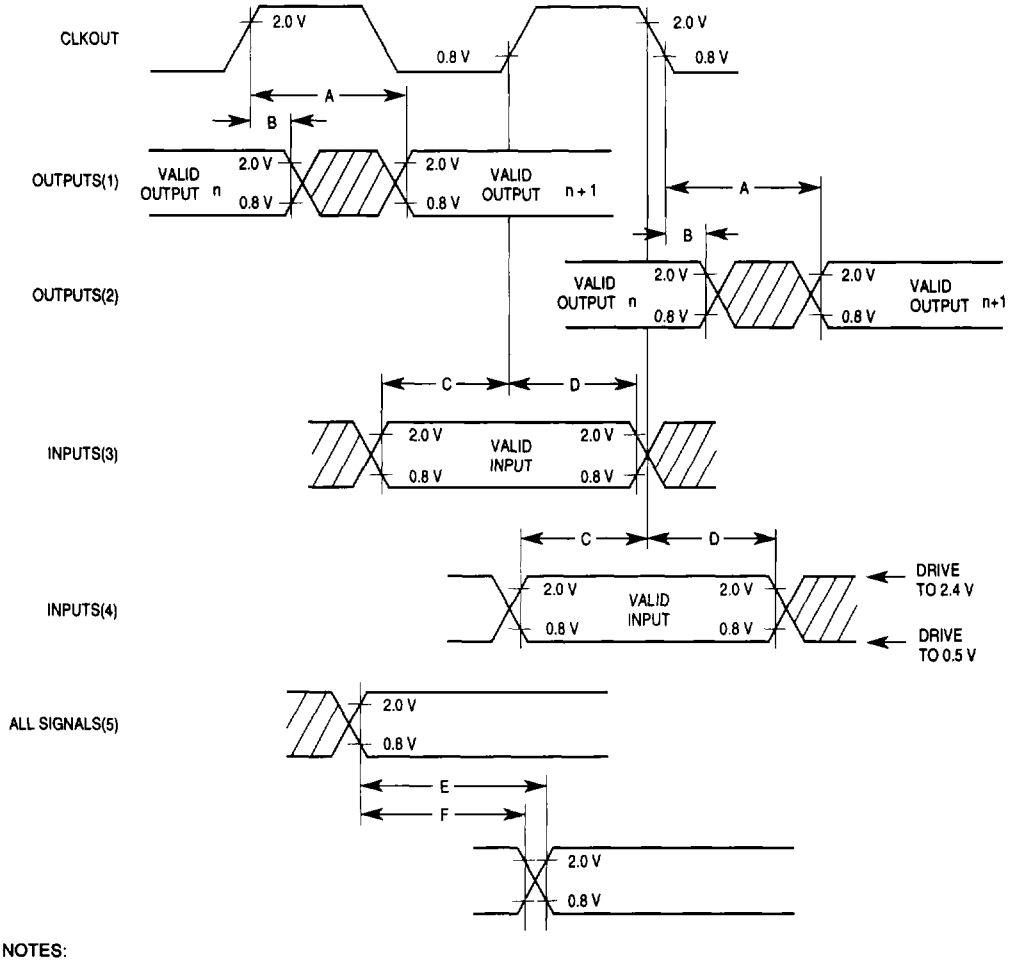
where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

10.4 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 10-1. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

Note that the testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 10-1. Drive Levels and Test Points for AC Specifications

10.5 DC Electrical Specifications

(GND = 0 Vdc, TA = 0 to 70°C; The electrical specifications in this document are preliminary; see numbered notes)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (except EXTAL)	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Input Low Voltage (3.3V Part Only; PA8-15, PB1, PC5, PC7 TCK)	V_{IL}	GND	0.5	V
Input Low Voltage (3.3V Part Only; All Other Pins)	V_{IL}	GND	0.8	V
EXTAL Input High Voltage	V_{IHC}	0.8•(V_{CC})	V_{CC}+0.3	V
Undershoot	—	—	–0.8	V
Input Leakage Current (All Input Only Pins except for TMS, TDI and TRST) V_{in} = V_{CC} or GND	I_{in}	–2.5	2.5	µA
Hi-Z (Off-State) Leakage Current (All Noncrystal Outputs and I/O Pins) V_{in} = 0.5/2.4 V	I_{OZ}	–20	20	µA
Signal Low Input Current V_{IL} = 0.8 V (TMS, TDI and TRST Pins Only) Signal High Input Current V_{IH} = 2.0 V(TMS, TDI and TRST Pins Only)	I_L IH	–0.5 –0.5	0.5 0.5	mA mA
Output High Voltage I_{OH} = –0.8 mA, V_{CC} = 4.75 V All Noncrystal Outputs Except Open Drain Pins	V_{OH}	2.4	—	V
Output Low Voltage (For 5 Volt Part) I_{OL} = 2.0 mACLKO1–2 ,FREEZE, IPIPE0–1, IFETCH, BKPTO I_{OL} = 3.2 mAA31–A0, D31–D0, FC3–0, SIZ0–1, PA0, 2, 4, 6, 8–15, PB0–5, PB8–17, PC0–11, TDO, PERR, PRTY0–3, IOUT0–2, AVECO, AS, CAS3–0, BLCRO, RAS0–7 I_{OL} = 5.3 mA, DSACK0–1, R/W, DS, OE, RMC, BG, BGACK, BERR I_{OL} = 7 mATXD1–4 I_{OL} =8.9 mAPB6, PB7, HALT, RESET, BR (Output)	V_{OL}	—	0.5 0.5 0.5 0.5 0.5	V
Output Low Voltage (For 3.3 volt part) I_{OL} = 2.0 mAA31–A0, FC3–0, SIZ0–1, D31–D0, PRTY0–3,CLKO1–2 ,FREEZE, IPIPE0–1, IFETCH, BKPTO I_{OL} = 3.2 mA PA0, 2, 4, 6, 8–15, PB0–5, PB8–17, PC0–11, TDO, PERR, PRTY0–3, IOUT0–2, AVECO, AS, CAS3–0, BLCRO, RAS0–7 I_{OL} = 5.3 mA, DSACK0–1, R/W, DS, OE, RMC, BG, BGACK, BERR I_{OL} = 7 mATXD1–4 I_{OL} =8.9 mAPB6, PB7, HALT, RESET, BR (Output)	V_{OL}	—	0.5 0.5 0.5 0.5 0.5	V
Input Capacitance All I/O Pins	C_{in}	—	20	pF
Load Capacitance (except CLKO1–2)	C_L	—	100	pF
Load Capacitance (CLKO1-2)	C_{Lc}		50	pF
Power (For 5 Volt Version)	Vcc	4.75	5.25	V
Power (For 3.3 Volt Version)	Vcc	3.0	3.6	V
Minimum Vcc Ramp up time on power on reset	^tRanp	4	—	mSec

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10.6 AC POWER DISSIPATION

Typical Curent Drain

Mode of Operation	Symbol	System Clock Frequency	BRGCLK Clock Frequency	SyncCLK Clock Frequency	Typ	Unit
Normal Mode (Rev A[1] and Rev B[2])	I_{DD}	25 MHz	25 MHz	25 MHz	250	ma
Normal Mode (Rev C[3] and Newer)	I_{DD}	25 MHz	25 MHz	25 MHz	237	ma
Normal Mode	I_{DD}	33 MHz	33 MHz	33 MHz	327	ma
Low Power Mode	I_{DDSB}	Divide by 2 12.5 MHz	Divide by 16 1.56 MHz	Divide by 2 12.5 MHz	150	ma
Low Power Mode	I_{DDSB}	Divide by 4 6.25 MHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	85	ma
Low Power Mode	I_{DDSB}	Divide by 16 1.56 MHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	35	ma
Low Power Mode	I_{DDSB}	Divide by 256 97.6 KHz	Divide by 16 1.56 MHz	Divide by 4 6.25 MHz	20	ma
Low Power Mode	I_{DDSB}	Divide by 256 97.6 KHz	Divide by 64 390 KHz	Divide by 64 390 KHz	13	ma
Low Power Stop VCO Off[5]	I_{DDSP}				0.5	ma
PLL Supply Current PLL Disabled PLL Enabled	I_{DDPD} I_{DDPE}				TBD TBD	

NOTES:
1. Rev A mask is C63T
2. Rev B masks are C69T, and F35G
3. Current Rev C masks are E63C, E68C and F15W
5. EXTAL frequency is 32KHz

All measurements was taken with only CLKO1 enabled, Vcc = 5.0V, V_{IL} = 0V and V_{IH} = Vcc

Maximum Power Dissipation

System Frequency	Vcc	Max P_D	Unit	Mask
25MHz	5.25 V	1.80	W	REV A[1] and REV B[2]
25MHz	5.25 V	1.45	W	REV C[3] and Newer
25MHz	3.6 V	0.65	W	REV C[3] and Newer
33MHz	5.25 V	2.00	W	REV C[3] and Newer

NOTES:
1. Rev A mask is C63T
2. Rev B masks are C69T, and F35G
3. Current Rev C masks are E63C, E68C and F15W

10.7 AC Electrical Specifications Control Timing

(GND = 0 Vdc, TA = 0 to 70°C; The electrical specifications in this document are preliminary; See Figure 10-2)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 25 MHz		5.0 V 33.34 MHz		Unit
			Min	Max	Min	Max	
	System Frequency	f_{sys}	dc[1]	25.00		33.34	MHz
	Crystal Frequency	f_{XTAL}	25	6000	25	6000	kHz
	On-Chip VCO System Frequency	f_{sys}	20	50	20	67	MHz
	Start-up Time With external clock (oscillator disabled) or after changing the multiplication factor MF.	t_{pll}		2500			clks
	CLKO1–2 stability	ΔCLK	TBD	TBD			%
1	CLKO1 Period	t_{cyc}	40	—	30	—	ns
1A	EXTAL Duty Cycle, MF	t_{dcyc}	40	60	40	60	%
1C	External Clock Input Period	t_{EXTcyc}	40	—	30	—	ns
2, 3	CLKO1 Pulse Width (Measured at 1.5v)	t_{CW1}	19	—	14	—	ns
2A, 3A	CLKO2 Pulse Width (Measured at 1.5v)	t_{CW2}	9.5	—	7	—	ns
4, 5	CLKO1 Rise and Fall Times (Full Drive)	t_{Crf1}	—	2	—	2	ns
4A, 5A	CLKO2 Rise and Fall Times (Full Drive)	t_{Crf2}	—	2	—	2	ns
5B	EXTAL to CLKO1 Skew—PLL enabled (MF<5)	t_{EXTP1}		a		a	ns
5C	EXTAL to CLKO2 Skew—PLL enabled (MF<5)	t_{EXTP2}		a		a	ns
5D	CLKO1 to CLKO2 Skew	t_{CSKW}		a		a	ns

Note: 1. Note that the minimum VCO frequency and the PLL default values put some restrictions on the minimum system frequency.

a: The following calculation should be used to determine the actual value for specifications 5B, 5C and 5D.

5B : 25Mhz +/-(0.9ns + 0.25 x (rise time)) (1.4ns@rise=2ns; 1.9ns@rise=4ns)

33Mhz +/-(0.5ns + 0.25 x (rise time)) (1ns@rise=2ns; 1.5ns@rise=4ns)

5C : 25/33Mhz +/-(2ns + 0.25 x (rise time)) (2.5ns@rise=2ns; 3ns@rise=4ns)

5D : 25Mhz +/-(3ns + 0.5 x (rise time)) (4ns@rise=2ns; 5ns@rise=4ns)

33Mhz +/-(2.5ns + 0.5 x (rise time)) (3.5ns@rise=2ns; 4.5ns@rise=4ns)

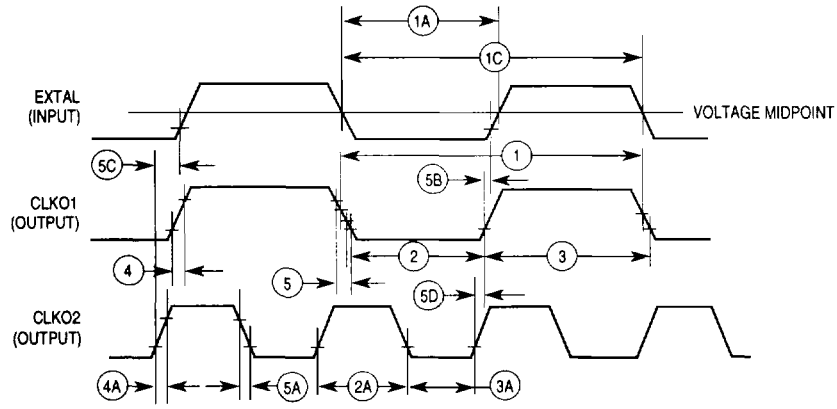


Figure 10-2. Clock Timing

10.8 EXTERNAL CAPACITOR FOR PLL

Characteristic	Symbol	3.3v		5.0 V		Unit
		Min	Max	Min	Max	
PLL external capacitor (XFC to VCCSYN)	c_{XFC}					
MF<5 (recommended value MF × 400 pF)		MFX680	MFX960	MFX340	MFX480	pF
MF>4 (recommended value MF × 540 pF)		MFX760	MFX1940	MFX380	MFX970	pF

Note: 1. MF – multiplication factor.

Examples:

1. MODCK1 pin = 0, MF = 1 ⇒ c_{XFC} = 400 pF
2. MODCK1 pin = 1, crystal is 32.768 KHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz, later on MF is changed to 762 to support a frequency of 25 MHz.

   Minimum c_{XFC} is: 762 x 380 = 289 nF, maximum c_{XFC} is: 401 x 970 = 390 nF. The recommended c_{XFC} for 25 MHz is: 762 x 540 = 414 nF.

   289 nF < c_{XFC} < 390 nF and closer to 414 nF. The proper available value for c_{XFC} is 390 nF.
3. MODCK1 pin = 1, crystal is 32.768 KHz (or 4.192 MHz), initial MF = 401, initial frequency = 13.14 MHz; later, MF is changed to 1017 to support a frequency of 33.34 MHz.

   Minimum c_{XFC} is: 1017 x 380 = 386 nF. Maximum c_{XFC} is: 401 x 970 = 390 nF ⇒ 386 nF < c_{XFC} < 390 nF.

   The proper available value for c_{XFC} is 390 nF.

3A. In order to get higher range, higher crystal frequency can be used (i.e. 50 KHz), in this case:

   Minimum c_{XFC} is: 667 x 380 = 253 nF. Maximum c_{XFC} is: 401 x 970 = 390 nF ⇒ 253 nF < c_{XFC} < 390 nF.

10.9 BUS OPERATION AC TIMING SPECIFICATIONS

(The electrical specifications in this document are preliminary; See Figure 10-3–Figure 10-19)

Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
6	CLKO1 High to Address, FC, SIZ, $\overline{RMC}$ Valid	t_{CHAV}	0	15	0	12	ns
6A	CLKO1 High to Address Valid (GAMX=1)	t_{CHAV}	0	20	0	15	ns
7	CLKO1 High to Address, Data, FC, SIZ, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	40	0	30	ns
8	CLKO1 High to Address, FC, SIZ, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	0	—	ns
9	CLKO1 Low to $\overline{AS}$, $\overline{DS}$, $\overline{OE}$, $\overline{WE}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{IACKx}$ Asserted	t_{CLSA}	3	20	3	15	ns
9[10]	CLKO1 Low to $\overline{CSx}$/$\overline{RASx}$ Asserted	t_{CLSA}	4	16	4	12	ns
9B[11]	CLKO1 High to $\overline{CSx}$/$\overline{RASx}$ Asserted	t_{CHCA}	4	16	4	12	ns
9A[2,10]	$\overline{AS}$ to $\overline{DS}$ or $\overline{CSx}$/$\overline{RASx}$ or $\overline{OE}$ Asserted (Read)	t_{STSA}	–6	6	-5.625	5.625	ns
9C[2,11]	$\overline{AS}$ to $\overline{CSx}$/$\overline{RASx}$ Asserted	t_{STCA}	14	26	9	21	ns
11[10]	Address, FC, SIZ, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CSx}$/$\overline{RASx}$, $\overline{OE}$, $\overline{WE}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	10	—	8	—	ns
11A[11]	Address, FC, SIZ, $\overline{RMC}$ Valid to $\overline{CSx}$/$\overline{RASx}$ Asserted	t_{AVCA}	30	—		—	ns
12[12]	CLKO1 Low to $\overline{AS}$, $\overline{DS}$, $\overline{OE}$, $\overline{WE}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{IACKx}$ Negated	t_{CLSN}	3	20	3	15	ns
12[16]	CLKO1 Low to $\overline{CSx}$/$\overline{RASx}$ Negated	t_{CLSN}	4	16	4	12	ns
12A[13,16]	CLKO1 High to $\overline{CSx}$/$\overline{RASx}$ Negated	t_{CHCN}	4	16	4	12	ns
12B	CS negate to WE negate (CSNTQ=1)	t_{CSTW}	15	—	12	—	ns
13[12]	$\overline{AS}$, $\overline{DS}$, $\overline{CSx}$, $\overline{OE}$, $\overline{WE}$, $\overline{IACKx}$ Negated to Address, FC, SIZ Invalid (Address Hold)	t_{SNAI}	10	—	7.5	—	ns
13A[13]	$\overline{CSx}$ Negated to Address, FC, SIZ Invalid (Address Hold)	t_{CNAI}	30	—		—	ns
14[10,12]	$\overline{AS}$, $\overline{CSx}$, $\overline{OE}$, $\overline{WE}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	75	—		—	ns
14C[11,13]	$\overline{CSx}$ Width Asserted	t_{CWA}	35	—		—	ns
14A	$\overline{DS}$ Width Asserted (Write)	t_{SWAW}	35	—		—	ns
14B	$\overline{AS}$, $\overline{CSx}$, $\overline{OE}$, $\overline{WE}$, $\overline{IACKx}$ (and $\overline{DS}$ Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	35	—		—	ns
14D[13]	$\overline{CSx}$ Width Asserted (Fast Termination Cycle)	t_{CWDW}	15	—	10	—	ns
15[3,10,12]	$\overline{AS}$, $\overline{DS}$, $\overline{CSx}$, $\overline{OE}$, $\overline{WE}$ Width Negated	t_{SN}	35	—		—	ns
16	CLKO1 High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	40	—	30	ns
17[12]	$\overline{AS}$, $\overline{DS}$, $\overline{CSx}$, $\overline{WE}$ Negated to R/$\overline{W}$ High	t_{SNRN}	10	—	7.5	—	ns
17A[13]	$\overline{CSx}$ Negated to R/$\overline{W}$ High	t_{CNRN}	30	—		—	ns
18	CLKO1 High to R/$\overline{W}$ High	t_{CHRH}	0	20	0	15	ns
20	CLKO1 High to R/$\overline{W}$ Low	t_{CHRL}	0	20	0	15	ns
21[10]	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CSx}$, $\overline{OE}$ Asserted	t_{RAAA}	10	—	7.5	—	ns

10.9 BUS OPERATION AC TIMING SPECIFICATIONS (CONTINUED)

Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
21A[11]	R/$\overline{W}$ High to $\overline{CSx}$ Asserted	t_{RACA}	30	—		—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RASA}	47	—	36	—	ns
23	CLKO1 High to Data-Out, Parity-Out Valid	t_{CHDO}	—	23	—	15	ns
23A	CLKO1 High to parity Valid	t_{CHPV}	—	25	—	15	ns
23B	Parity Valid to $\overline{CAS}$ low	t_{PVCL}	3	—	3	—	ns
24[12]	Data-Out, Parity-Out Valid to Negating Edge of $\overline{AS}$, $\overline{CSx}$, $\overline{WE}$, (Fast Termination Write)	t_{DVASN}	10	—	7.5	—	ns
25[12]	$\overline{DS}$, $\overline{CSx}$, $\overline{WE}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold)	t_{SNDOI}	10	—	7.5	—	ns
25A[13]	$\overline{CSx}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold)	t_{CNDOI}	35	—	25	—	ns
26	Data-Out, Parity-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DVSA}	10	—	7.5	—	ns
27[15]	Data-In, Parity-In to CLKO1 Low (Data Setup)	t_{DICL}	1	—	1	—	ns
27B[14]	Data-In, Parity-In Valid to CLKO1 Low (Data Setup)	t_{DICL}	20	—	15	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ Asserted to CLKO1 Low (Setup Time)	t_{BELCL}	10	—	7.5	—	ns
28[18]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$ Negated	t_{SNDN}	0	50	0	37.5	ns
29[4]	$\overline{DS}$, $\overline{CSx}$, $\overline{OE}$ Negated to Data-In, Parity-In Invalid (Data-In, Parity-In Hold)	t_{SNDI}	0	—	0	—	ns
29A[4]	$\overline{DS}$, $\overline{CSx}$, $\overline{OE}$ Negated to Data-In High Impedance	t_{SHDI}	—	40	—	30	ns
30[4]	CLKO1 Low to Data-In, Parity-In Invalid (Fast Termination Hold)	t_{CLDI}	10	—	7.5	—	ns
30A[4]	CLKO1 Low to Data-In High Impendance	t_{CLDH}	—	60	—	45	ns
31[5,15]	$\overline{DSACKx}$ Asserted to Data-In, Parity-In Valid	t_{DADI}	—	32	—	24	ns
31A	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	t_{DADV}	—	10	—	7.5	ns
31B[5,14]	$\overline{DSACKx}$ Asserted to Data-In, Parity-In Valid	t_{DADI}	—	35	—	26	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{HRf}	—	140	—		ns
33	CLKO1 High to $\overline{BG}$ Asserted	t_{CLBA}	—	20	—	15	ns
34	CLKO1 High to $\overline{BG}$ Negated	t_{CLBN}	—	20	22.5	15	ns
35[6]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	1	—	CLKO1
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2.5	1	2.5	CLKO1
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	2	—	CLKO1
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	1	—	CLKO1
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	100	—	75	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Termination Write or Read)	t_{RWAS}	75	—	56	—	ns
47A	Asynchronous Input Setup Time	t_{AIST}	5	—	4	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	10	—	7.5	—	ns

10.9 BUS OPERATION AC TIMING SPECIFICATIONS (CONTINUED)

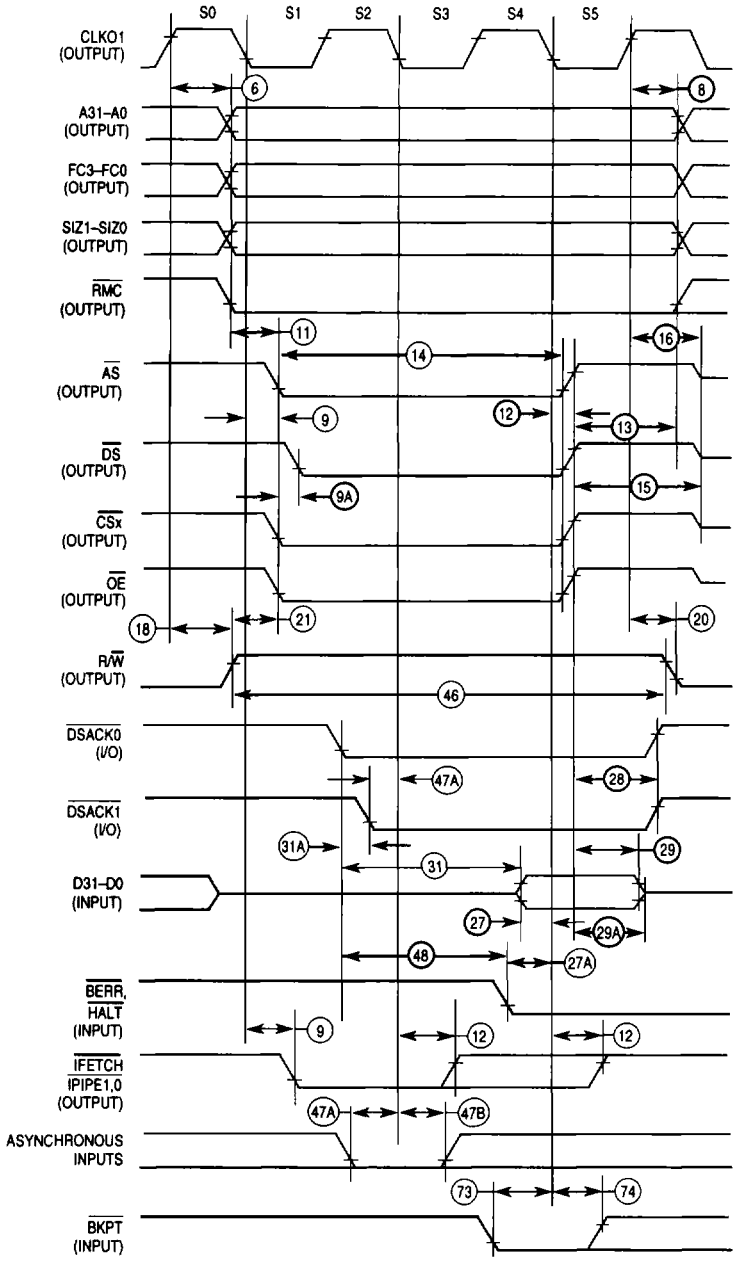
Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
48[5,7]	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	t_{DABA}	—	30	—	22.5	ns
49	CLKO1 high to $\overline{BERR}$, $\overline{RESETS}$, $\overline{RESETH}$ output Low	t_{CHRO}	—	—	—	—	ns
53	Data-Out, Parity-Out Hold from CLKO1 High	t_{DOCH}	0	—	0	—	ns
54	CLKO1 High to Data-Out, Parity-Out High Impedance	t_{CHDH}	—	20	—	15	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	25	—	19	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	—	512	—	CLKO1
56A	$\overline{RESET}$ Pulse Width (Input from External Device)	t_{RPWI}	20	—	20	—	CLKO1
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	0	—	ns
58	CLKO1 High to $\overline{BERR}$, $\overline{RESETS}$, $\overline{RESETH}$ Driven Low	t_{CHBRL}	—	30		26	ns
58A	CLKO1 Low to $\overline{RESETS}$ Driven Low (upon Reset Instruction execution only)	t_{CLRL}	—	30		26	ns
60	CLKO1 High to $\overline{BCLRO}$ Asserted	t_{CHBCA}	—	20	—	15	ns
61	CLKO1 High to $\overline{BCLRO}$ Negated	t_{CHBCN}	—	20	—	15	ns
62[9]	$\overline{BR}$ Synchronous Setup Time	t_{BRSU}	5	—	3.75	—	ns
63[9]	$\overline{BR}$ Synchronous Hold Time	t_{BRH}	10	—	7.5	—	ns
64[9]	$\overline{BGACK}$ Synchronous Setup Time	t_{BGSU}	5	—	3.75	—	ns
65[9]	$\overline{BGACK}$ Synchronous Hold Time	t_{BGH}	10	—	7.5	—	ns
66	$\overline{BR}$ low to CLKO1 Rising Edge (040 comp. mode)	t_{BRCH}	5	—	5	—	ns
70	CLKO1 Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	30	0	22.5	ns
71	Data Setup Time to CLKO1 Low (Show Cycle)	t_{SCLDS}	10	—	7.5	—	ns
72	Data Hold from CLKO1 Low (Show Cycle)	t_{SCLDH}	6	—	3.75	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	10	—	7.5	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	6	—	3.75	—	ns
75	$\overline{RESETH}$ Low to Config2–0, MOD1–0, B16M valid	t_{MST}	—	500	—	500	CLKO1
76	Config2–0	t_{MSH}	0	—	0	—	ns
77	MOD1–0 Hold Time, B16M Hold Time	t_{MSH}	10	—	10	—	CLKO1
80	DSI Input Setup Time	t_{DSISU}	10	—	7.5	—	ns
81	DSI Input Hold Time	t_{DSIH}	6	—	3.75	—	ns
82	DSCLK Setup Time	t_{DSCSU}	10	—	7.5	—	ns
83	DSCLK Hold Time	t_{DSCH}	6	—	3.75	—	ns
84	DSO Delay Time	t_{DSOD}	—	t_{cyc}+ 20	—	tcyc+ 20	ns
85	DSCLK Cycle	t_{DSCCYC}	2	—	2	—	CLKO1
86	CLKO1 High to Freeze Asserted	t_{FRZA}	0	35	0	26.25	ns
87	CLKO1 High to Freeze Negated	t_{FRZN}	0	35	0	26.25	ns

10.9BUS OPERATION AC TIMING SPECIFICATIONS (CONTINUED

Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
88	CLKO1 High to $\overline{IFETCH}$ High Impedance	t_{IFZ}	0	35	0	26.25	ns
89	CLKO1 High to $\overline{IFETCH}$ Valid	t_{IF}	0	35	0	26.25	ns
90	CLKO1 High to $\overline{PERR}$ Asserted	t_{CHPA}	0	20	0	15	ns
91	CLKO1 High to $\overline{PERR}$ Negated	t_{CHPN}	0	20	0	15	ns
92	Minimum Vcc Ramp-Up Time At Power-On Reset	t_{RMIN}	5	-	5	-	ms

NOTES:
1. All AC timing is shown with respect to 0.8 V and 2.0 V levels unless otherwise noted.
2. This number can be reduced to 5 ns if strobes have equal loads.
3. If multiple chip selects are used, the $\overline{CSx}$ width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
4. These hold times are specified with respect to $\overline{DS}$ or $\overline{CSx}$ on asynchronous reads and with respect to CLKO1 on fast termination reads. The user is free to use either hold time for fast termination reads.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DSACKx}$ low to data setup time (#31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKO1 low setup time (#27) for the following clock cycle: $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to CLKO1 low setup time (#27A) for the following clock cycle.
6. To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.
7. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (#47).
8. During interrupt acknowledge cycles, the processor may insert up to two wait states between states S0 and S1.
9. These specs are for Synchronous Arbitration only. ASTM=1.
10. These $\overline{CSx}$ specs are for TRLX=0. If $\overline{RASx}$ and $\overline{RASxDD}$ are connected together, reduce max value of $\overline{RASx}$ specification by 1.5ns.
11. These $\overline{CSx}$ specs are for TRLX=1. If $\overline{RASx}$ and $\overline{RASxDD}$ are connected together, reduce max value of $\overline{RASx}$ specification by 1.5ns.
12. These $\overline{CSx}$ specs are for CSNTQ=0.
13. These $\overline{CSx}$ specs are for CSNTQ=1; or $\overline{RASx}$ specs for DRAM accesses.
14. These specs are read cycles with parity check and PBEE=1.
15. These specs are read cycles with parity check and PBEE=0,PAREN=1.
16. These $\overline{RASx}$ specs are for page miss case.
17. These specifications only apply to $\overline{CSx}$/$\overline{RASx}$ pins.
18. This specification applies to non fast termination cycles. In fast termination cycles, the $\overline{BERR}$ signal must be negated by 20ns after negation of $\overline{AS}$, $\overline{DS}$.

10



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-3. Read Cycle

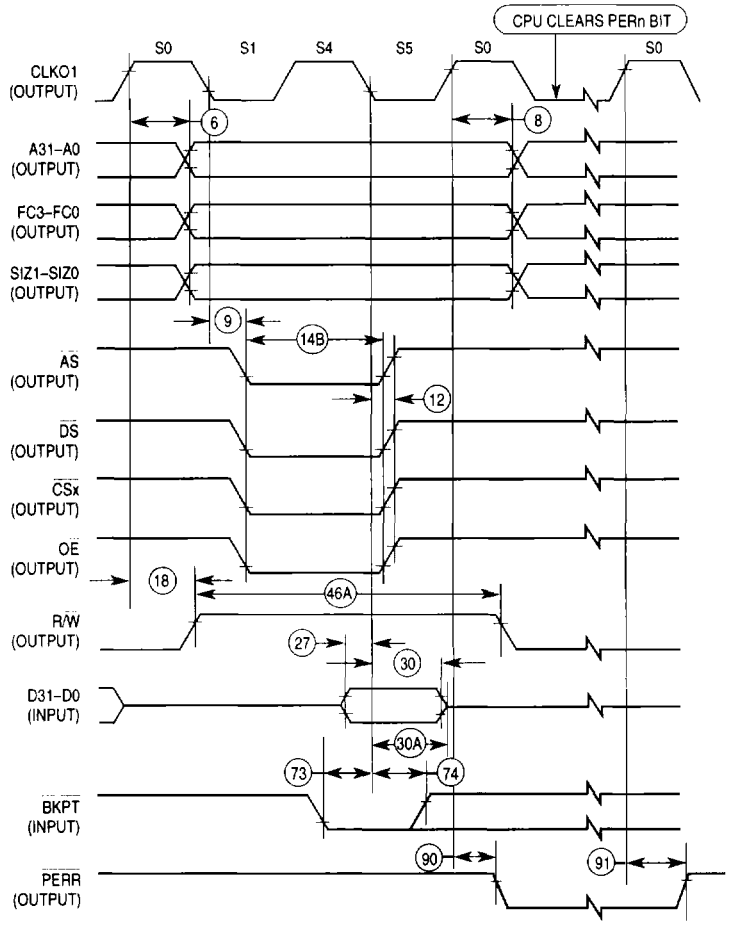
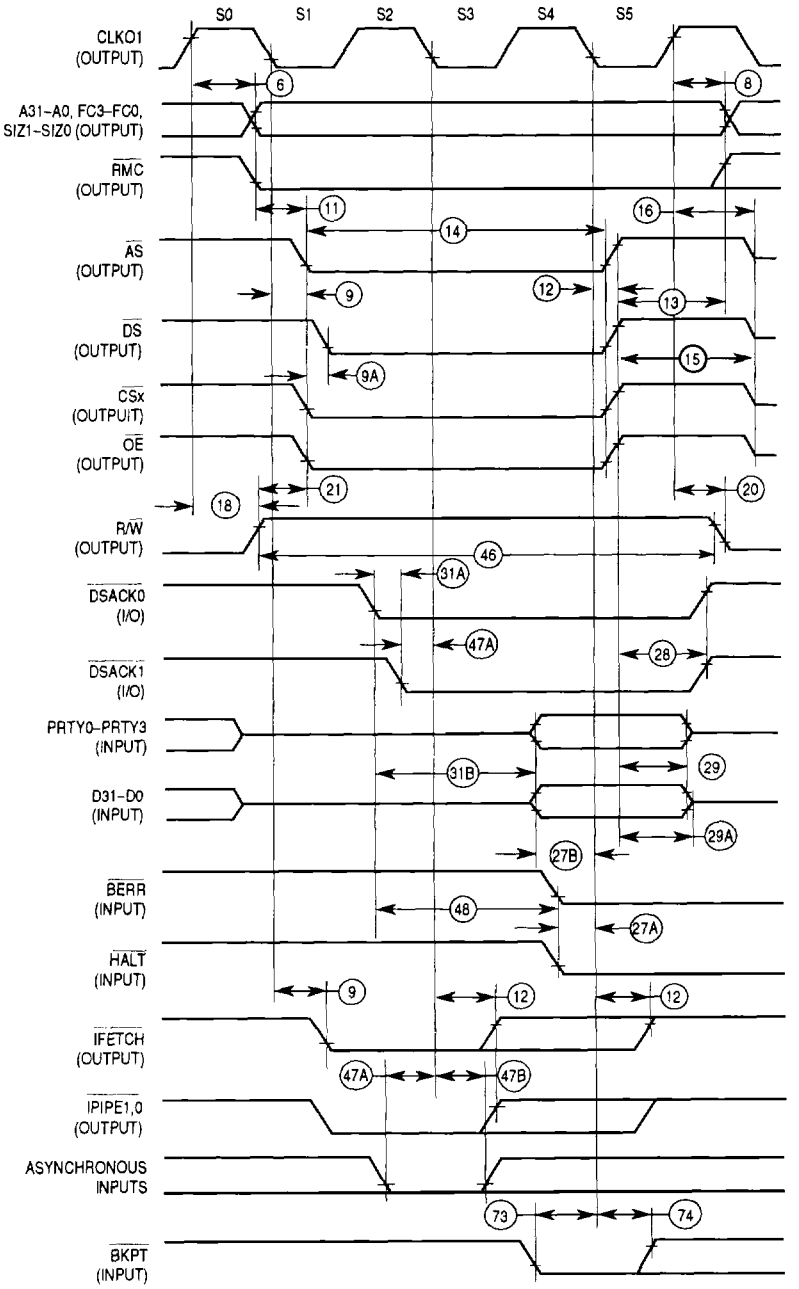


Figure 10-4. Fast Termination Read Cycle (Parity Check PAREN = 1, PBEE = 0)



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-5. Read Cycle (With Parity Check, PBEE = 1)

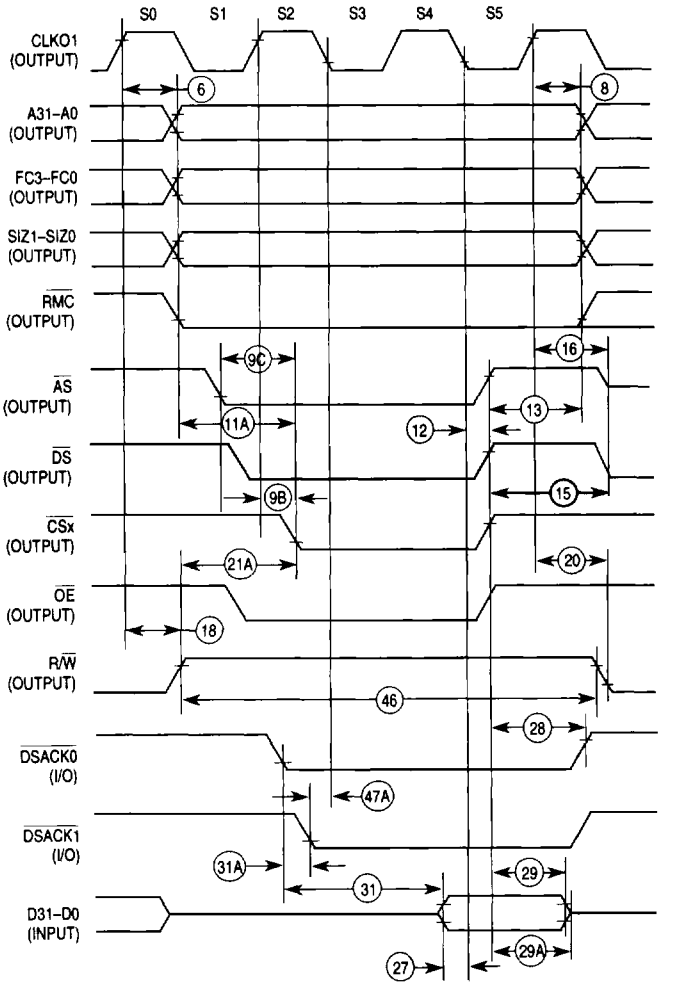
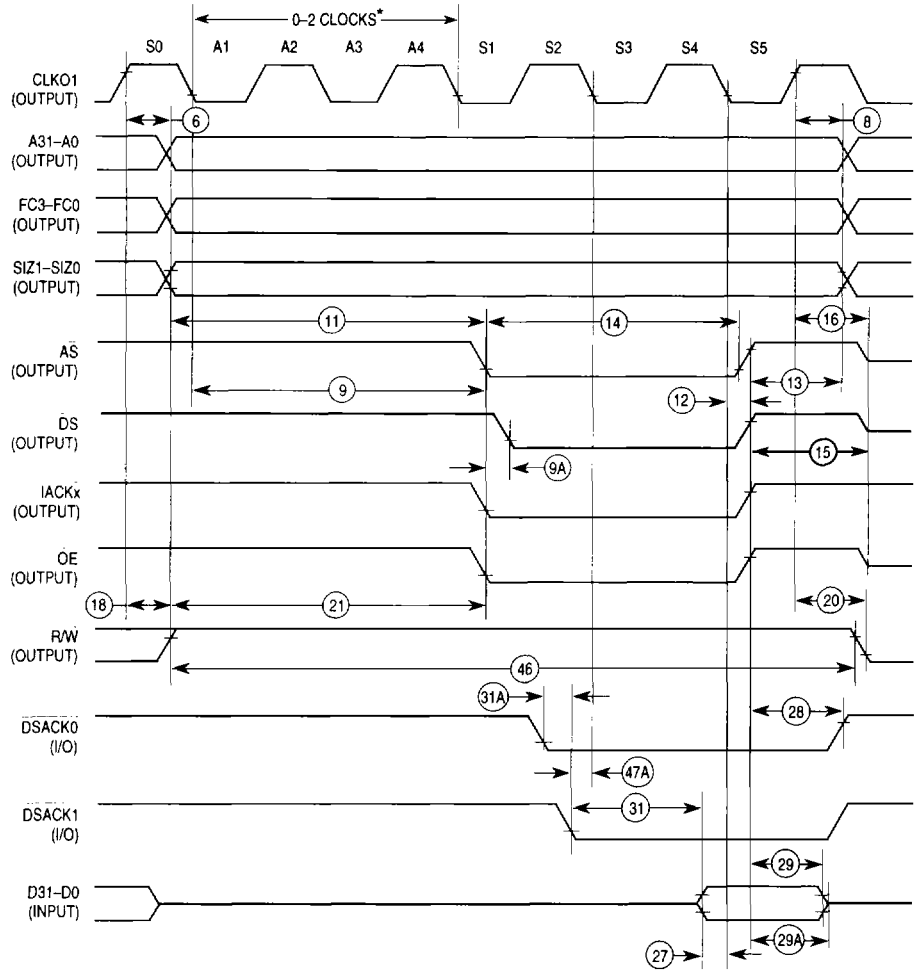


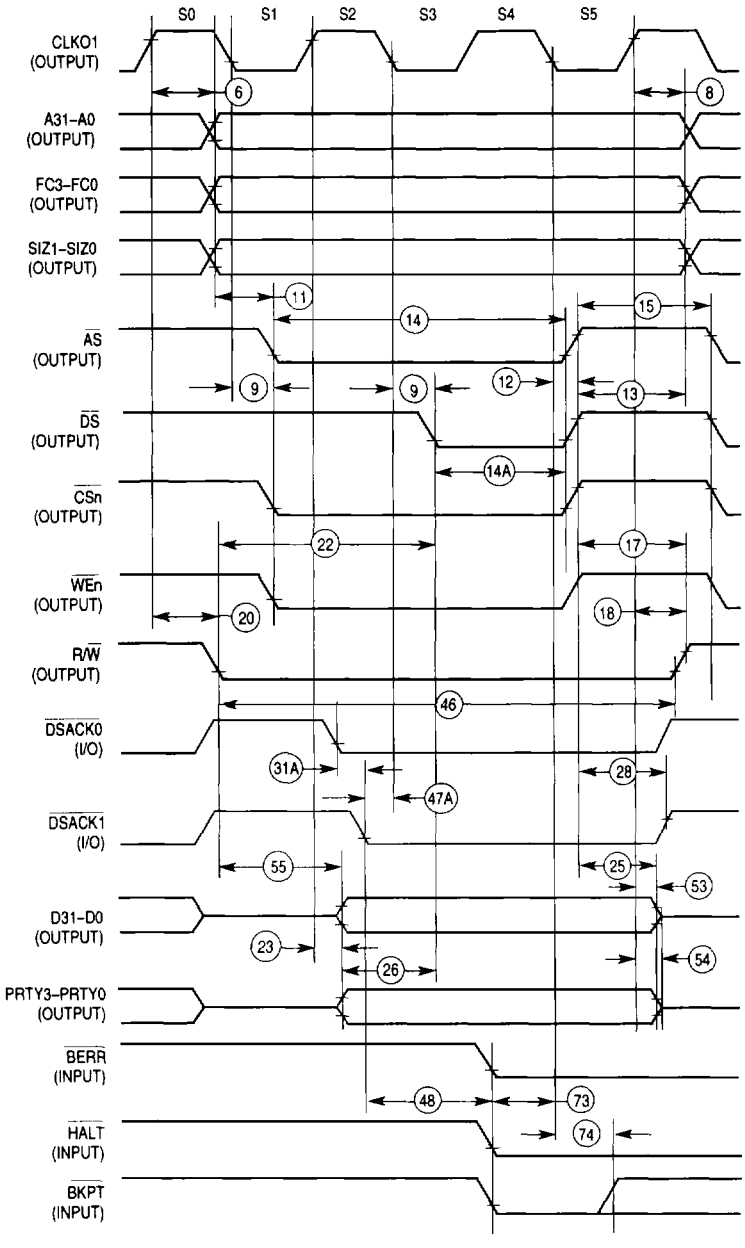
Figure 10-6. SRAM: Read Cycle (TRLX = 1)



*Up to two wait states may be inserted by the processor between states S0 and S1.

Figure 10-7. CPU32+ IACK Cycle

10



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-8. Write Cycle

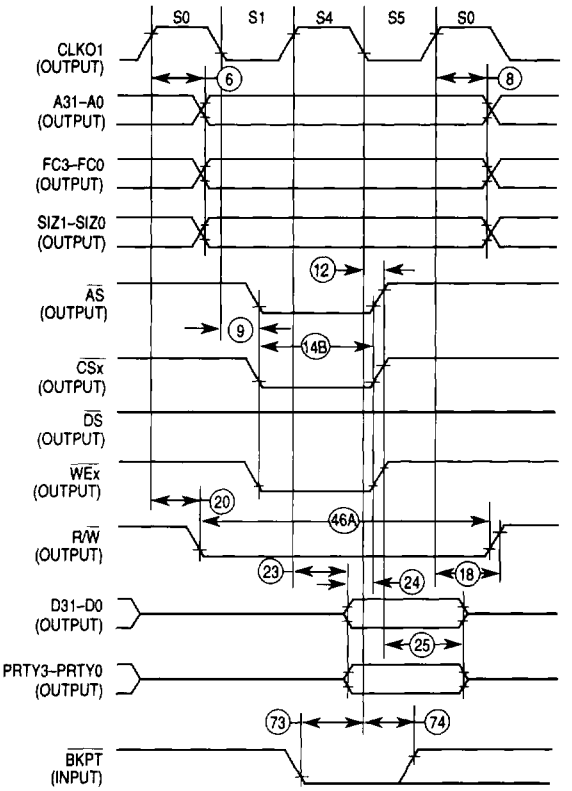


Figure 10-9. Fast Termination Write Cycle

10

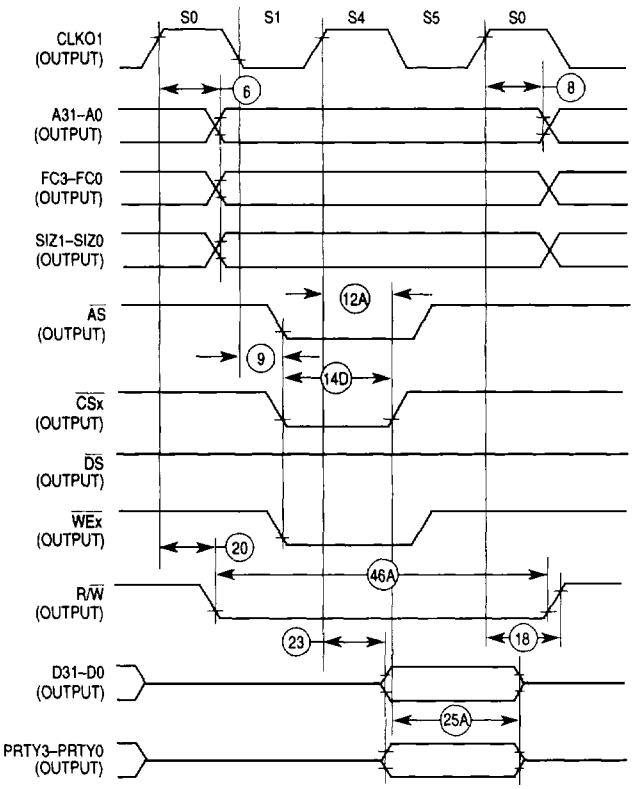
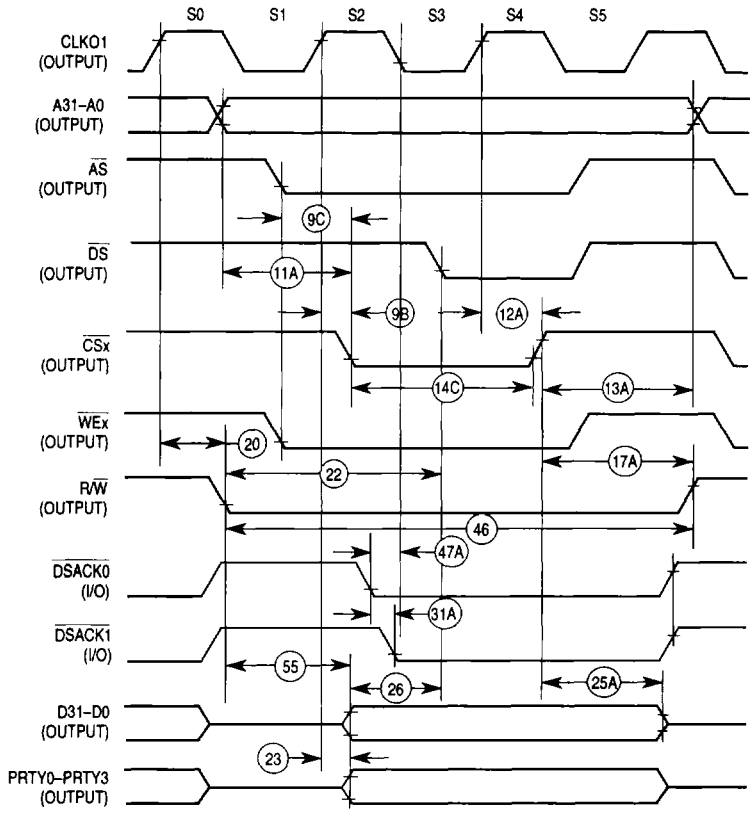


Figure 10-10. SRAM: Fast Termination Write Cycle (CSNTQ = 1)

10



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-11. SRAM: Write Cycle (TRLX = 1, CSNTQ = 1, TCYC = 0)

10

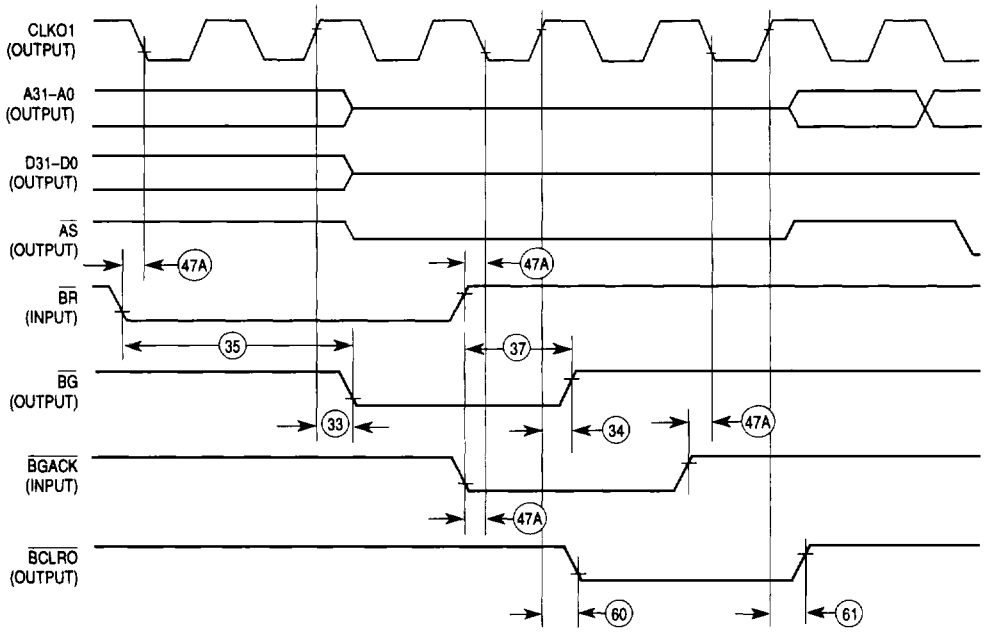


Figure 10-12. ASYNC Bus Arbitration – IDLE Bus Case

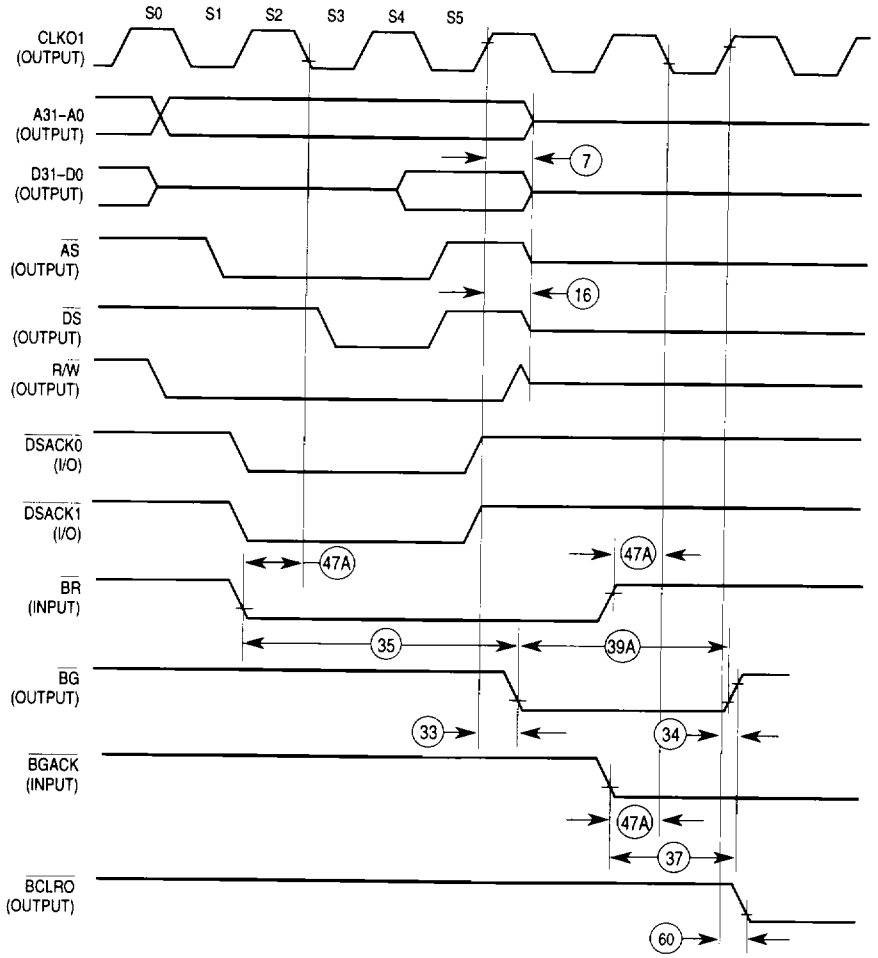


Figure 10-13. ASYNC Bus Arbitration – Active Bus Case

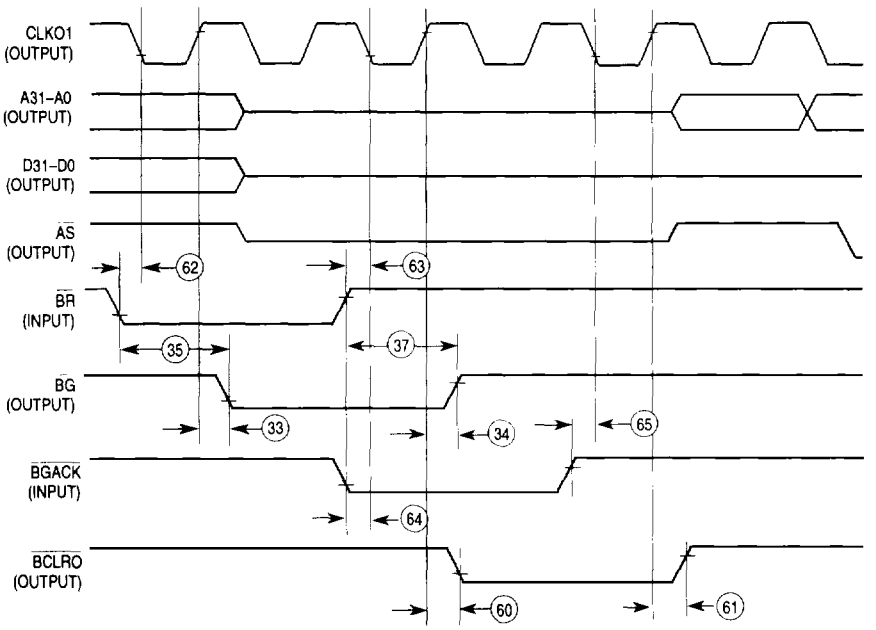


Figure 10-14. SYNC Bus Arbitration – IDLE Bus Case

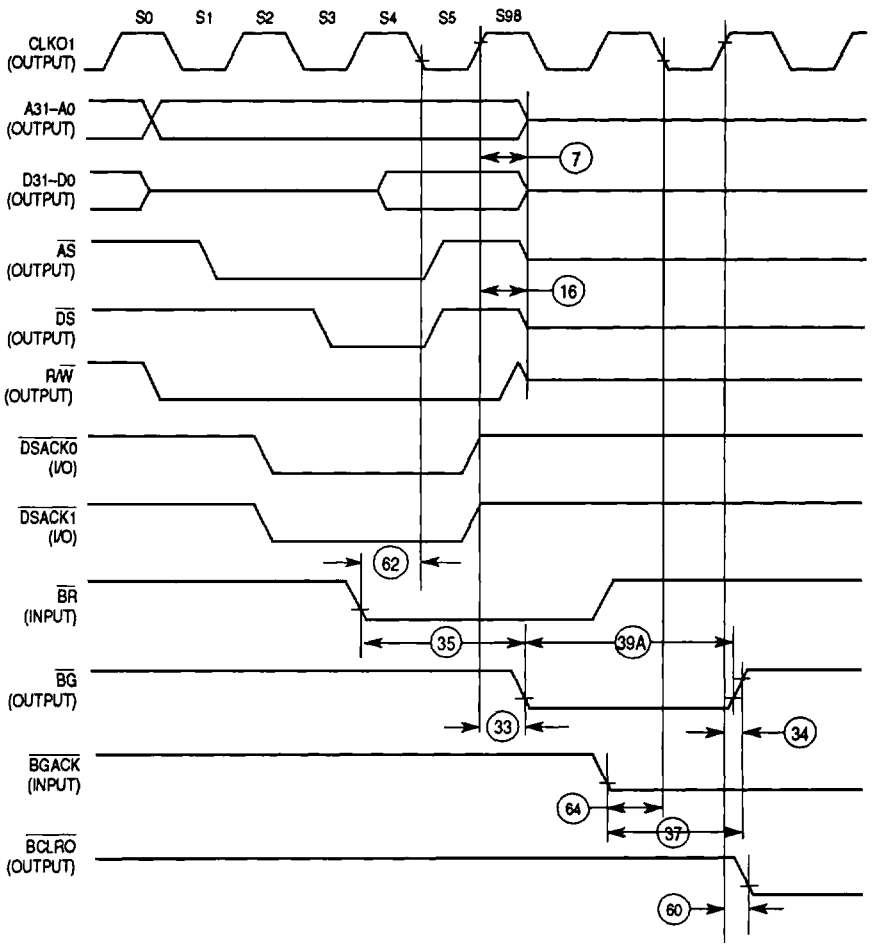


Figure 10-15. SYNC Bus Arbitration – Active Bus Case

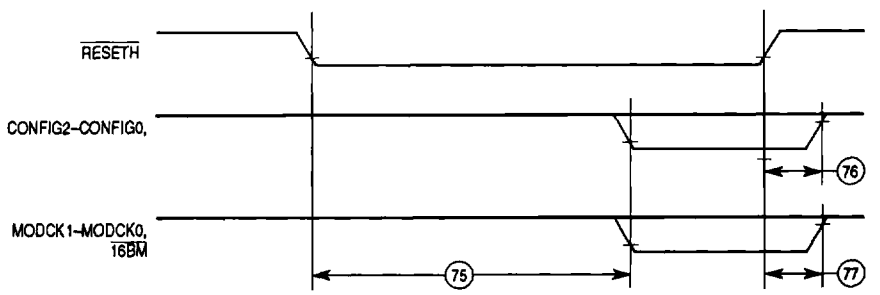


Figure 10-16. Configuration And Clock Mode Select Timing

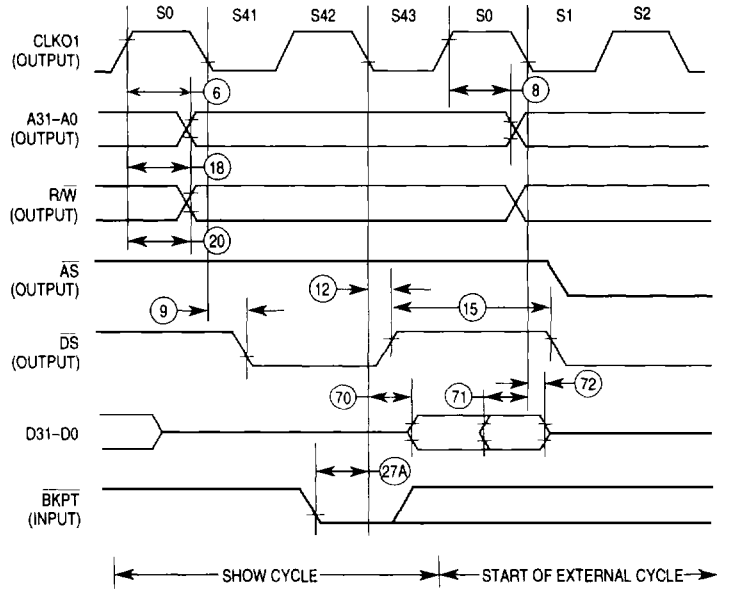


Figure 10-17. Show Cycle

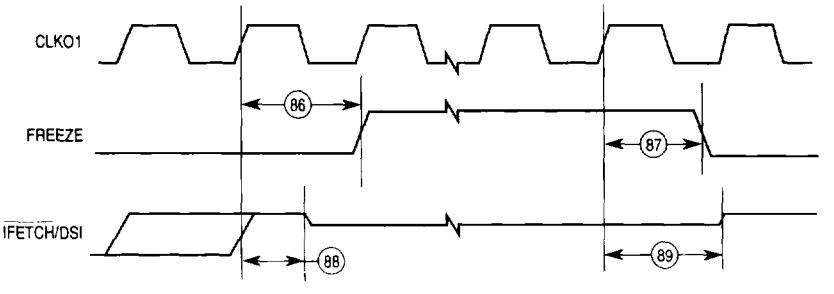


Figure 10-18. Background Debug Mode FREEZE Timing

10

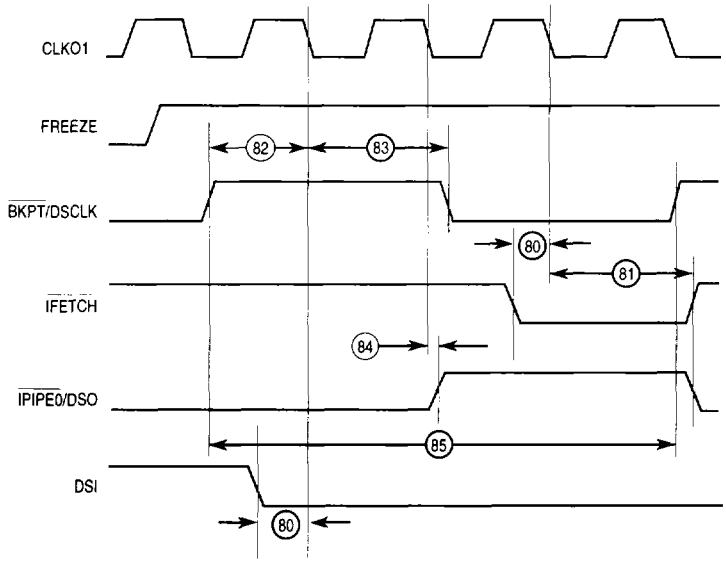


Figure 10-19. Background Debug Mode Serial Port Timing

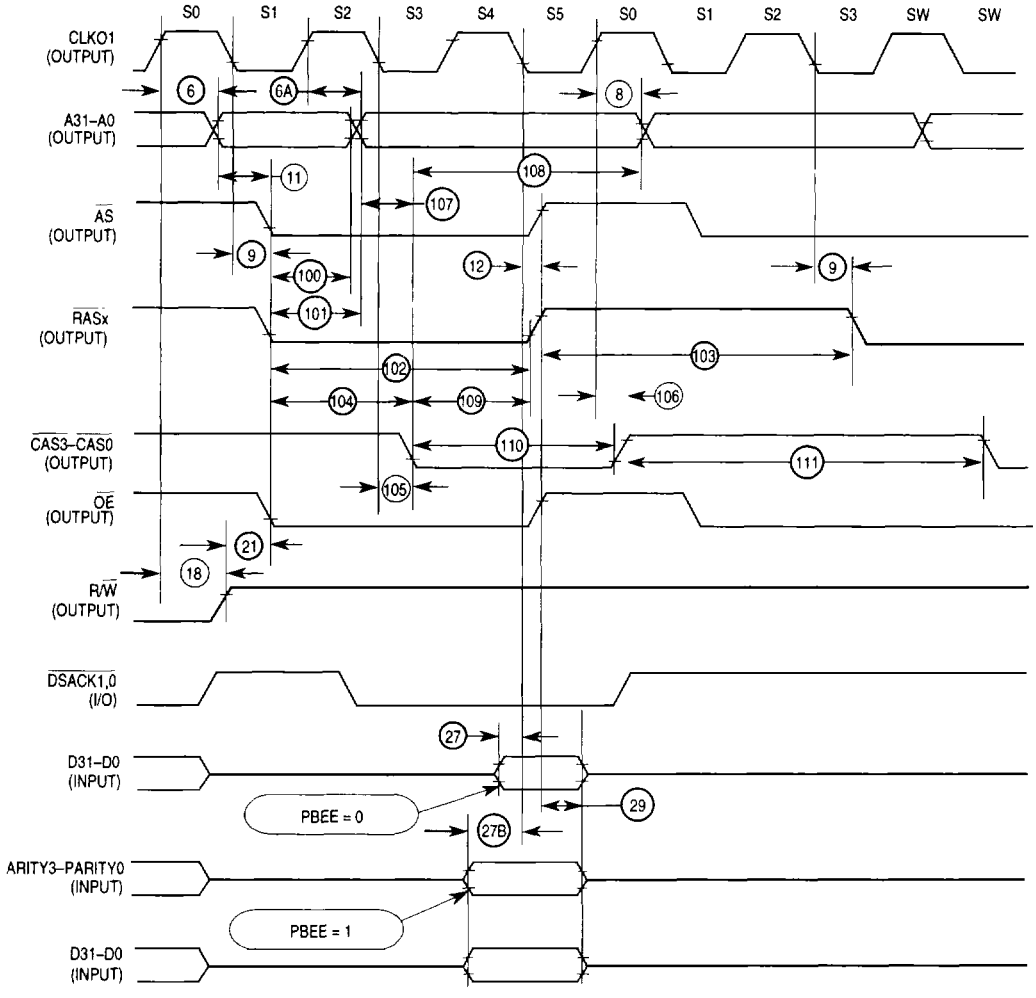
10.10 BUS OPERATION—DRAM ACCESSES AC TIMING SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-20–Figure 10-24.)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
100	$\overline{RASx}$ Asserted to Row Address Invalid	15		11.25		ns
101	$\overline{RASx}$ Asserted to Column Address Valid	20		15		ns
102	$\overline{RASx}$ Width Asserted	75		56.25		ns
103[1]	$\overline{RASx}$ Width Negated (Back to Back Cycles)	75		56.25		ns
104	$\overline{RASx}$ Asserted to $\overline{CASx}$ Asserted	35		26.25		ns
105	CLKO1 Low to $\overline{CASx}$ Asserted	3	13	2	10	ns
105A	CLKO1 High to $\overline{CASx}$ Asserted (Refresh Cycle)	3	13	2	10	ns
106	CLKO1 High to $\overline{CASx}$ Negated	3	13	2	10	ns
107	Column Address Valid to $\overline{CASx}$ Asserted	15		11.25		ns
108	$\overline{CASx}$ Asserted to Column Address Negated	40		30		ns
109	$\overline{CASx}$ Asserted to $\overline{RASx}$ Negated	35		27		ns
110	$\overline{CASx}$ Width Asserted	50		37.5		ns
111[1]	$\overline{CASx}$ Width Negated (Back to Back Cycles)	95		71.25		ns
111A	$\overline{CASx}$ Width Negated (Page Mode)	20		15		ns
113	$\overline{WE}$ Low to $\overline{CASx}$ Asserted	35		27		ns
114	$\overline{CASx}$ Asserted to $\overline{WE}$ Negated	35		27		ns
115	R/$\overline{W}$ Low to $\overline{CASx}$ Asserted (Write)	75		56.25		ns
116	$\overline{CASx}$ Asserted to R/$\overline{W}$ High (Write)	55		41.25		ns
117	Data-Out, Parity-Out Valid to $\overline{CASx}$ Asserted	10		7.5		ns
119	CLKO1 High to AMUX Negated	3	16	2	12	ns
120	CLKO1 High to AMUX Asserted	3	16	2	12	ns
121	AMUX High to $\overline{RASx}$ Asserted	15		11.25		ns
122	$\overline{RASx}$ Asserted to AMUX Low	15		11.25		ns
123	AMUX Low to $\overline{CASx}$ Asserted	15		11.25		ns
124	$\overline{CASx}$ Asserted to AMUX High	55		41.25		ns
125	$\overline{RAS}$/$\overline{CASx}$ Negated to R/W change	0		0		ns

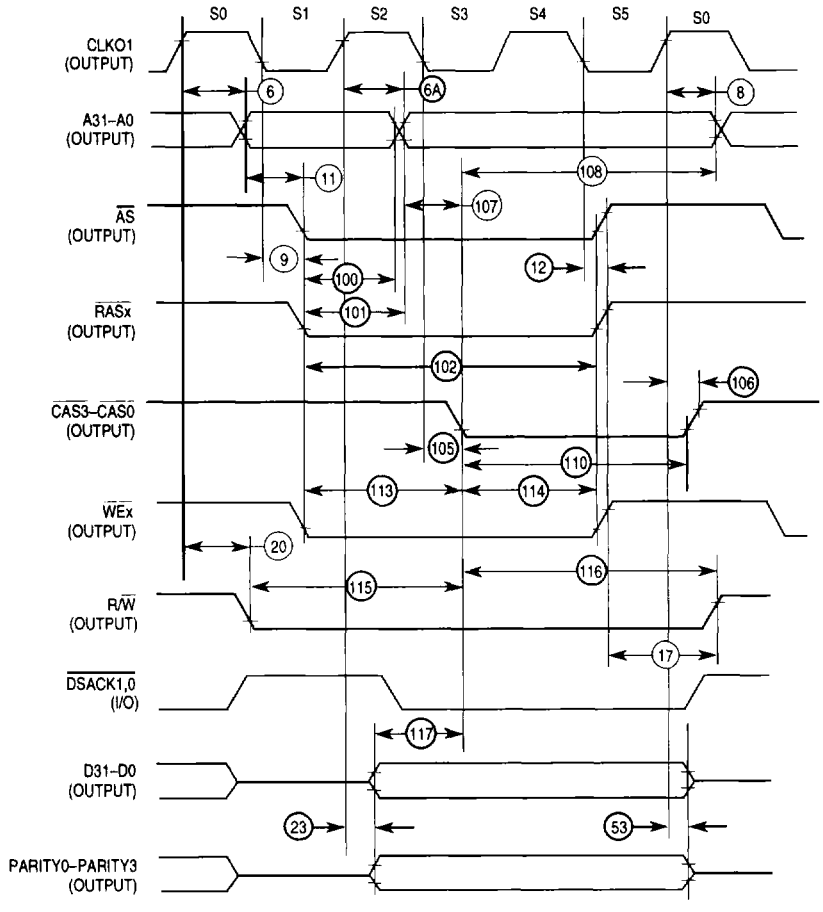
NOTES:
1.This specification is for WBTQ=0, when WBTQ=1 add another clock.

10



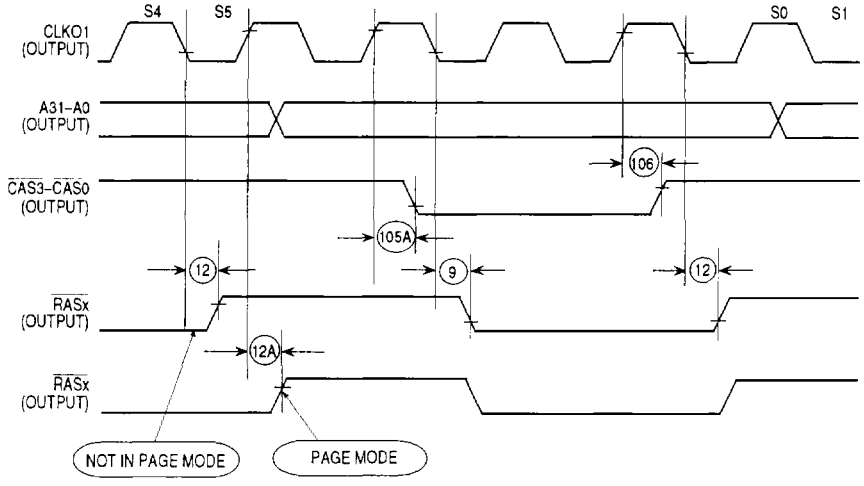
NOTE: All timing is shown with respect 0.8-V AND 2.0-V levels.

Figure 10-20. DRAM: Normal Read Cycle (Internal Mux, TRLX = 0)



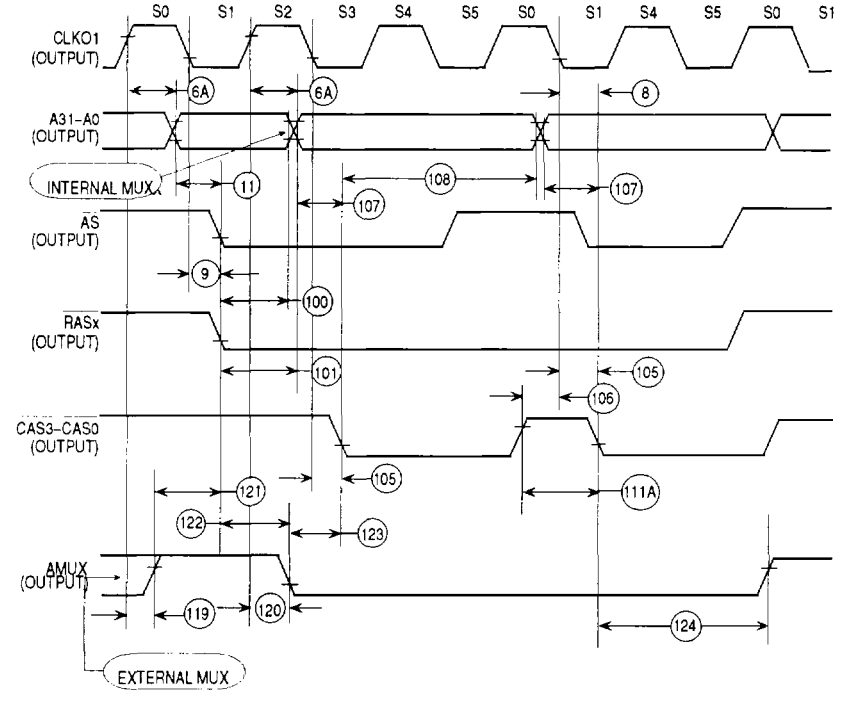
NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-21. DRAM: Normal Write Cycle



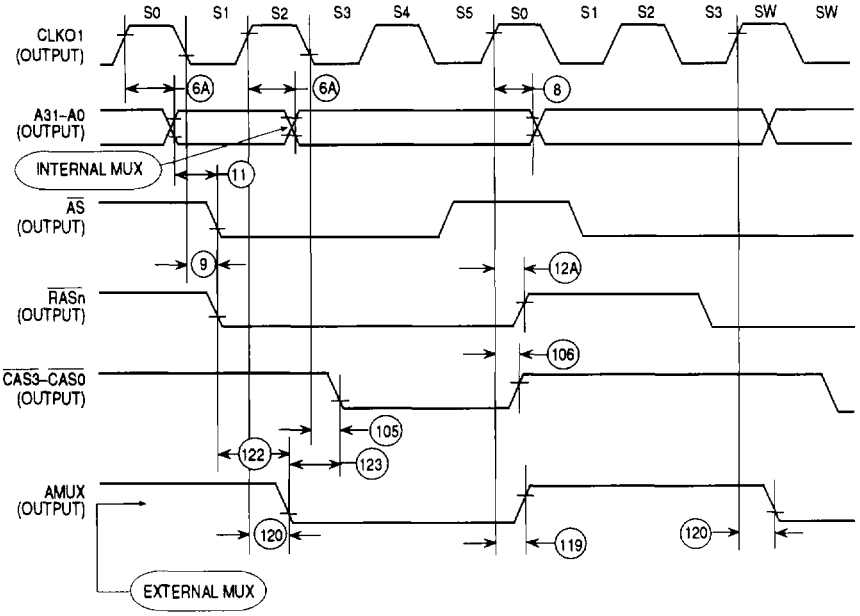
NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-22. DRAM: Refresh Cycle



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-23. DRAM: Page-Mode—Page-Hit



NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 10-24. DRAM: Page-Mode—Page-Miss

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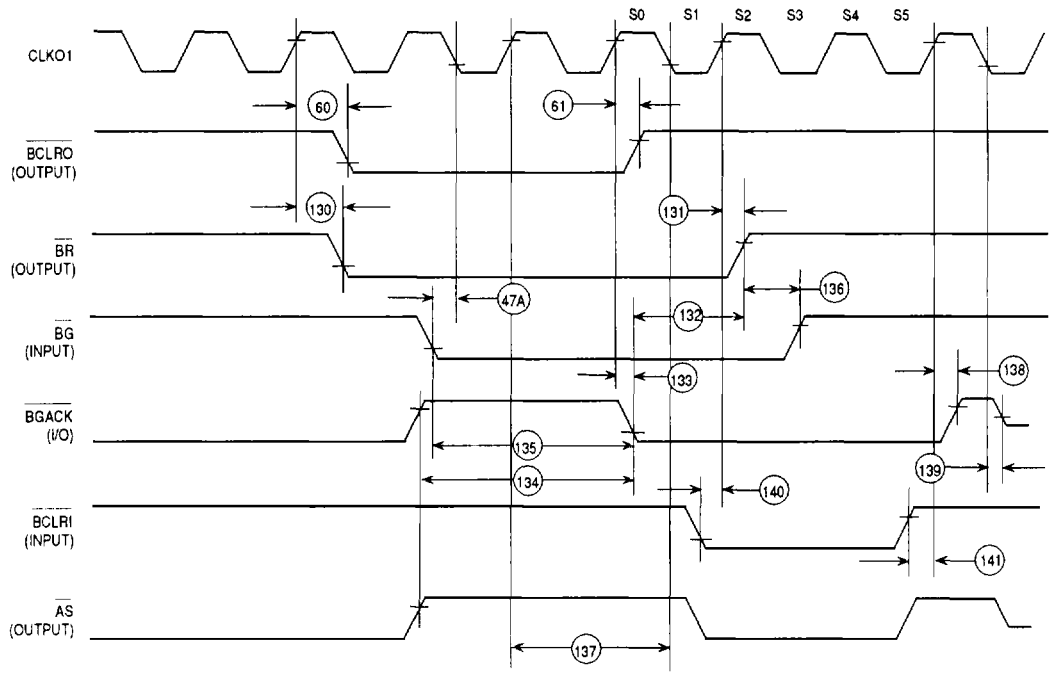
10.11 030/QUICC BUS TYPE SLAVE MODE BUS ARBITRATION AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-25 and Figure 10-26)

Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
130[1]	CLKO1 High to $\overline{BR}$ Asserted	—	20	—	15	ns
131	CLKO1 High to $\overline{BR}$ High Impedence	—	20	—	15	ns
132[1]	$\overline{BGACK}$ Low to $\overline{BR}$ High Impedence	20	—	15	—	ns
133	CLKO1 High to $\overline{BGACK}$ Asserted	—	20	—	15	ns
134[2]	$\overline{AS}$ and $\overline{BGACK}$ High (the latest one) to $\overline{BGACK}$ Low (when $\overline{BG}$ is asserted)	1.5	2.5 + 20	1.5	2.5 +15	clks ns
135[1,2]	$\overline{BG}$ Low to $\overline{BGACK}$ Low (no other Bus Master)	1.5	2.5 + 20	1.5	2.5 +15	clks ns
137	Clock on which $\overline{BGACK}$ Low to Clock on which $\overline{AS}$ Low.	0	—	0	—	clks
138	CLKO1 High to $\overline{BGACK}$ High	—	20	—	15	ns
139	CLKO1 Low to $\overline{BGACK}$ High Impedance	—	15	—	11.25	ns
140	$\overline{BCLRI}$ Low to CLKO1 High	15	—	11.25	—	ns
141	$\overline{BCLRI}$ High to CLKO1 High	15	—	11.25	—	ns
142[3]	$\overline{BG}$ Low to CLKO1 Low	15	—	11.25	—	ns
143[3]	$\overline{AS}$ and $\overline{BGACK}$ High (the latest one) to $\overline{BGACK}$ Low (when $\overline{BG}$ is asserted)	1	1 + 20	1	1 +15	clks ns
144[1,3]	$\overline{BG}$ Low to $\overline{BGACK}$ Low (no other bus master)	1	1 + 20	1	1 +15	clks ns

NOTES:
1. Specifications are for asynchronous arbitration (ASTM=0).
2. Specifications are for synchronous arbitration (ASTM=1).

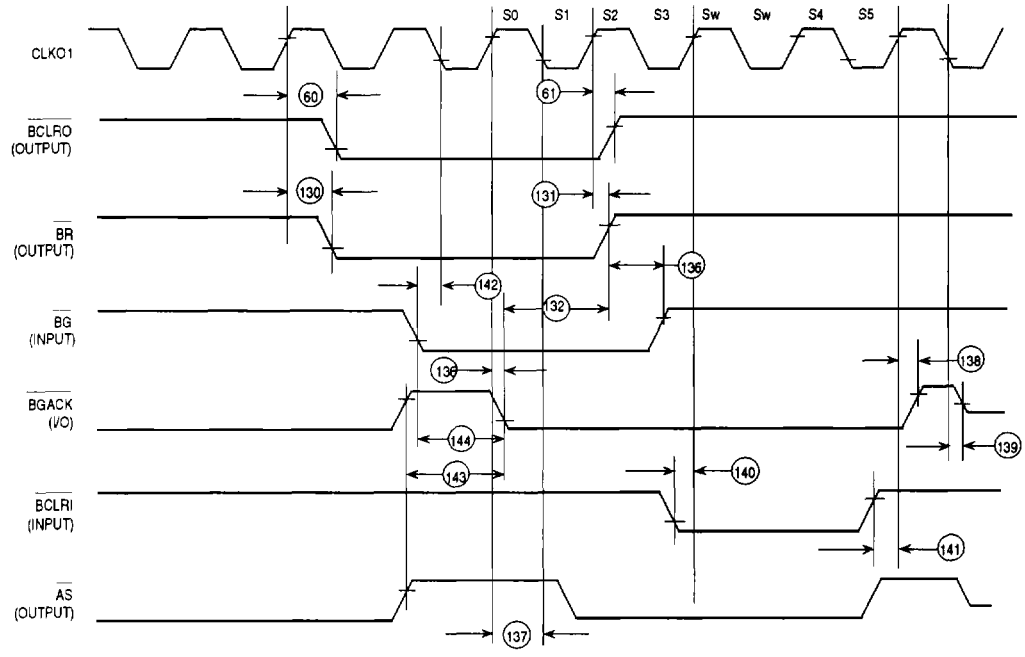
10



NOTE: Diagram does not apply to MC68040 companion mode.

Figure 10-25. MC68360 Slave Mode Asynchronous Arbitration

10



NOTE: Diagram does not apply to MC68040 companion mode.

Figure 10-26. MC68360 Slave Mode Synchronous Arbitration

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10.12 030/QUICC BUS TYPE SLAVE MODE INTERNAL READ/WRITE/ IACK ASYNCHRONOUS CYCLES AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-27 and Figure 10-28)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
150	Address Valid to $\overline{AS}$ Low	10	—	8	—	ns
151	$\overline{AS}$ Valid to $\overline{DS}$ Low	0	—	0	—	ns
152	$\overline{AS}$ inactive Time	1	—	1	—	clk
153	$\overline{AS}$ High to Address Hold Time	0	—	0	—	ns
154	$\overline{DS}$ Inactive to $\overline{AS}$ Inactive	0	—	0	—	ns
155	$\overline{DS}$ Inactive Time	1	—	1	—	clk
156	$\overline{DSACK}$ Low to $\overline{AS}$, $\overline{DS}$ High	0	—	0	—	ns
157	Data Out Valid to $\overline{DSACK}$ Low	—	15	—	11.25	ns
158	CLKO1 Low to Data-Out Valid	—	20	—	15	ns
159	$\overline{DS}$ High to Data-Out Hold Time	0	—	0	—	ns
160	$\overline{DS}$ High to Data High Impedance	—	40	—	30	ns
161	CLKO1 High to $\overline{DSACK}$ Low (Note 2)	—	20	—	15	ns
161A	CLKO1 High to $\overline{DSACK}$ Low (Note 3)	—	25			ns
162	$\overline{AS}$ High to $\overline{DSACK}$ High	—	20	—	15	ns
163	$\overline{DSACK}$ High to $\overline{DSACK}$ High Impedance	—	15	—	11.25	ns
164	R/$\overline{W}$ Valid to $\overline{DS}$ Low	0	—	0	—	ns
165	$\overline{DS}$ High To R/$\overline{W}$ High	0	—	0	—	ns
166	Data-In, $\overline{MBARE}$ Valid to $\overline{DS}$ Low	—	20	—	15	ns
167	$\overline{DSACK}$ Low to Data-In, $\overline{MBARE}$ Hold Time	0	—	0	—	ns
169	CLKO1 Low to $\overline{AVECO}$ Low	—	20	—	15	ns
170	$\overline{AS}$ High to $\overline{AVECO}$ High Impedance	—	30	—	23	ns
171	CLKO1 Low to $\overline{IACK}$ Low	—	20	—	15	ns
172	$\overline{AS}$ High to $\overline{IACK}$ High	—	30	—	23	ns

NOTES:
1Asynchronous specifications above are valid only when BSTM=0.
2. For external bus master to external memory or peripheral.
3. For external bus master to internal memory or registers.

10

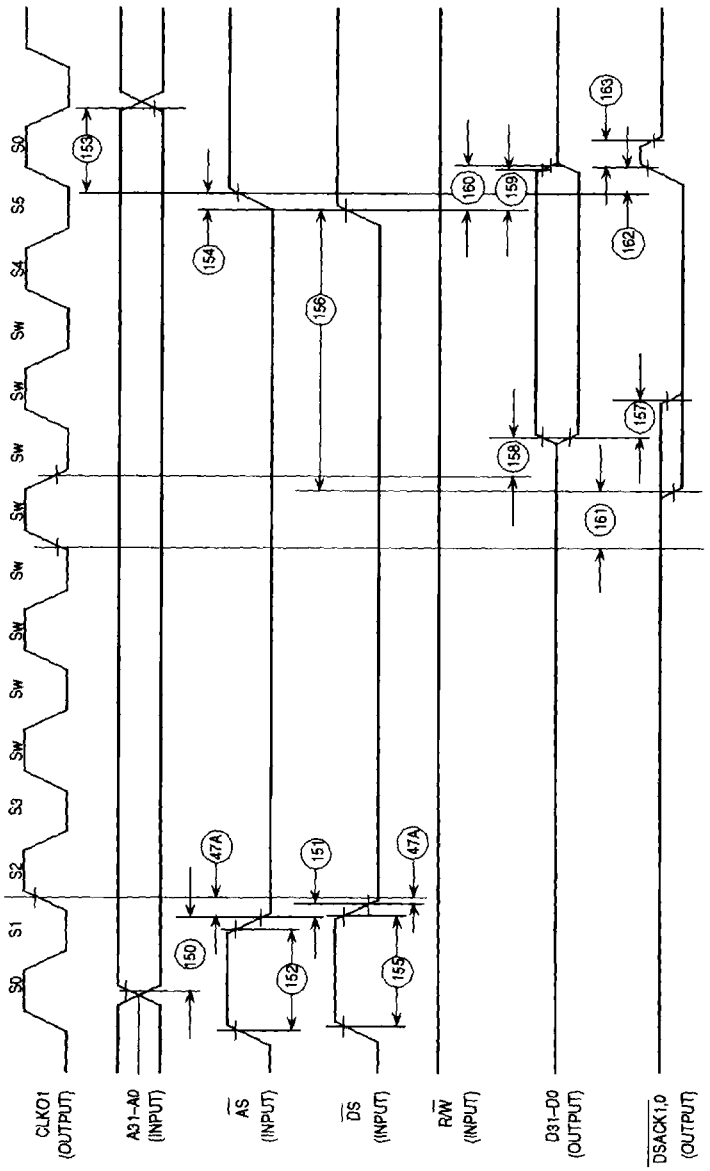

Figure 10-27. External MC68030/MC68360 Internal Asynchronous Read Cycle Timing Diagram

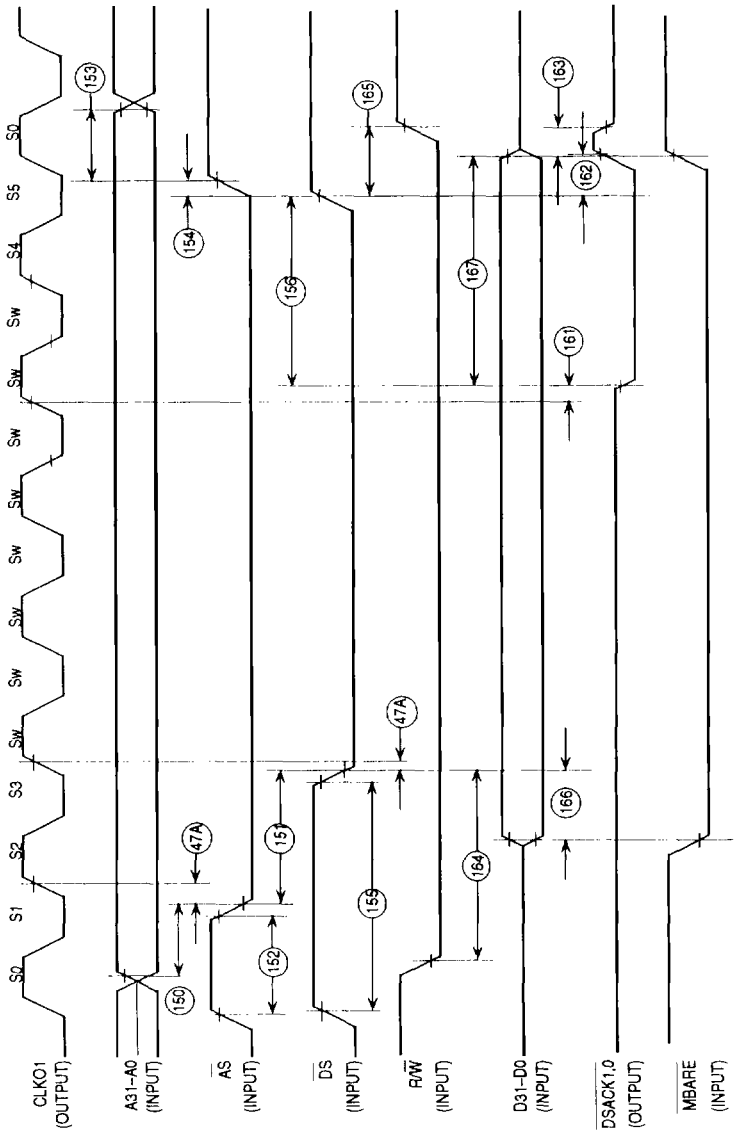

Figure 10-28. External MC68030/MC68360 Internal Registers Asynchronous Write Cycle Timing Diagram

10.13 030/QUICC BUS TYPE SLAVE MODE INTERNAL READ/WRITE/ IACK SYNCHRONOUS CYCLES AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figures 10-29–10-32.)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
180	$\overline{AS}$ Low to CLKO1 High	7	—	6	—	ns
181	CLKO1 Low to $\overline{AS}$ High	—	20	—	15	ns
182	$\overline{DS}$ Low to CLKO1 High	7	—	6	—	ns
183	CLKO1 Low to $\overline{DS}$ High	—	20	—	15	ns
184	CLKO1 Low to Data-Out Valid	—	20	—	15	ns
185	R/$\overline{W}$ Low to CLKO1 High	7	—	6	—	ns
186	CLKO1 High to R/$\overline{W}$ High	—	20	—	15	ns
187	Data-In, $\overline{MBARE}$ Valid to $\overline{DS}$ Low	2	—	2	—	ns
188	CLKO1 Low to Data-In, $\overline{MBARE}$ Hold Time	10	—	7.5	—	ns
191	$\overline{AS}$ Low to $\overline{AVECO}$ Low	—	30	—	23	ns
192	$\overline{AS}$ Low to $\overline{IACK}$ Low	—	30	—	23	ns

NOTES:
1Synchronous specifications above are valid only when BSTM=1.

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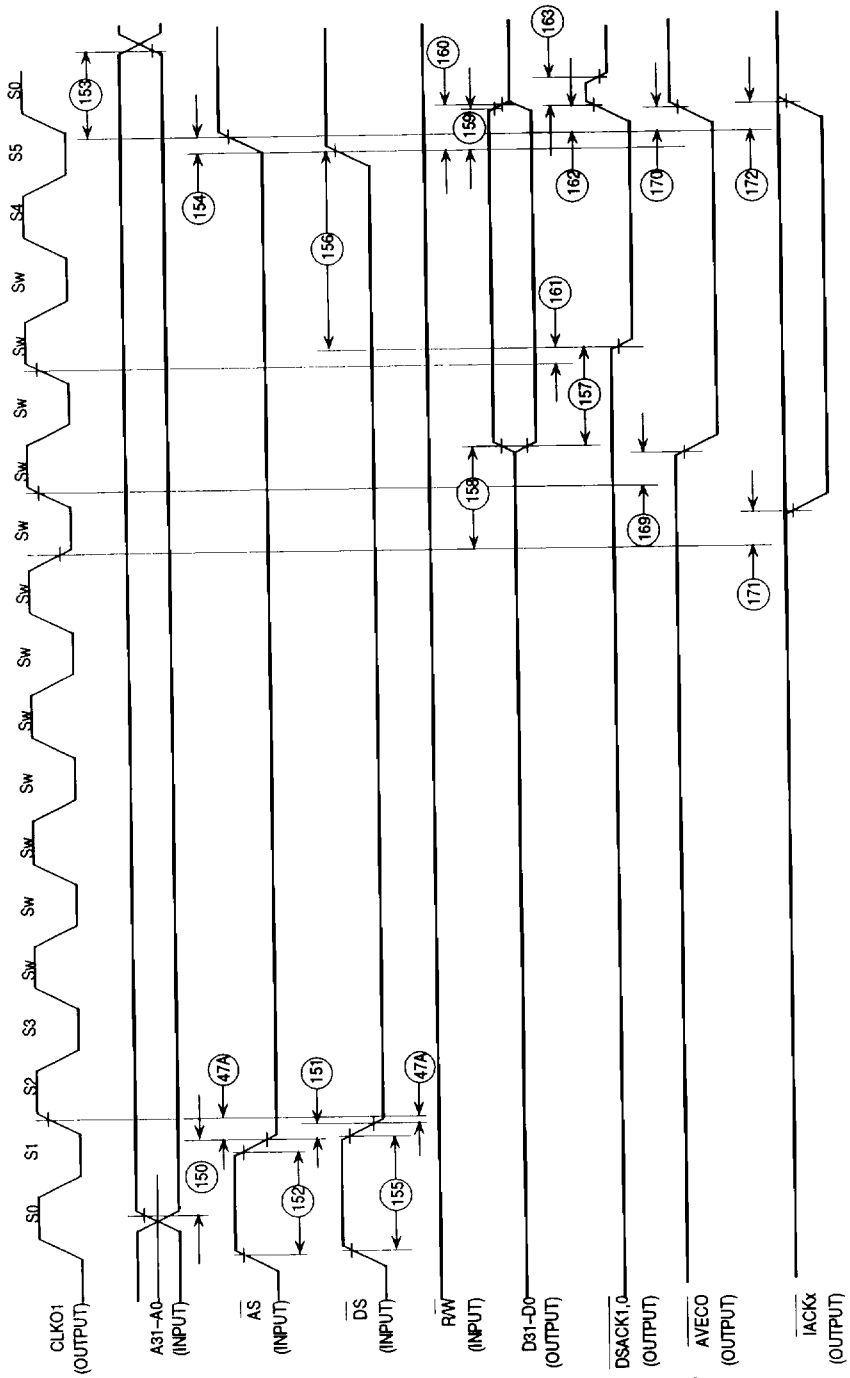
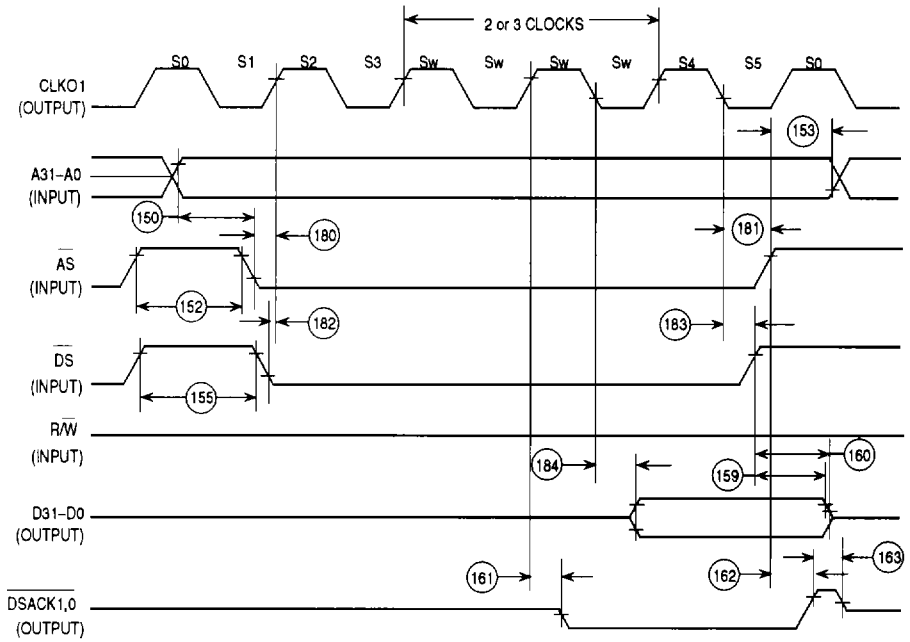


Figure 10-29. External MC68030/MC68360 Asynchronous IACK Cycle Timing Diagram

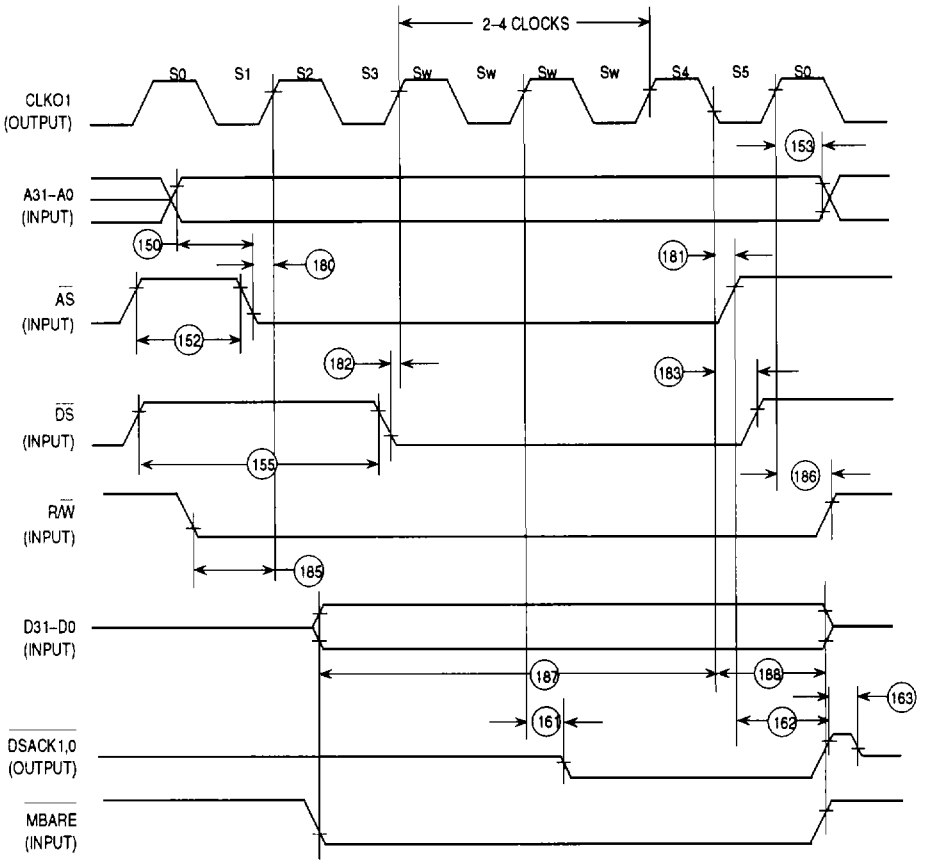
10



NOTE: Two wait states are inserted when reading the SIM, dual-port RAM, and CPM. Three wait states are inserted when reading the SI RAM. Additional wait states may be inserted when the SHEN1–SHEN0 =10 and one of the internal masters is accessing an internal peripheral.

Figure 10-30. External MC68030/MC68360 Internal Synchronous Read Cycle Timing Diagram

10



NOTE: Two wait states are inserted when writing to the SIM. Three wait states are inserted when writing to the dual-port RAM and CPM. Four wait states are inserted when writing the SI RAM. Additional wait states may be inserted when the SHEN1–SHEN0 = 10 and one of the internal masters is accessing an internal peripheral.

Figure 10-31. External MC68030/MC68360 Internal Synchronous Write Cycle Timing Diagram

NOTE

This figure represents an IACK cycle for both vectored and autovectored interrupt. If IACK is for a vectored interrupt, AVECO will not be driven. If IACK is an autovector interrupt, DSACK0-1 and data bus will not be driven.

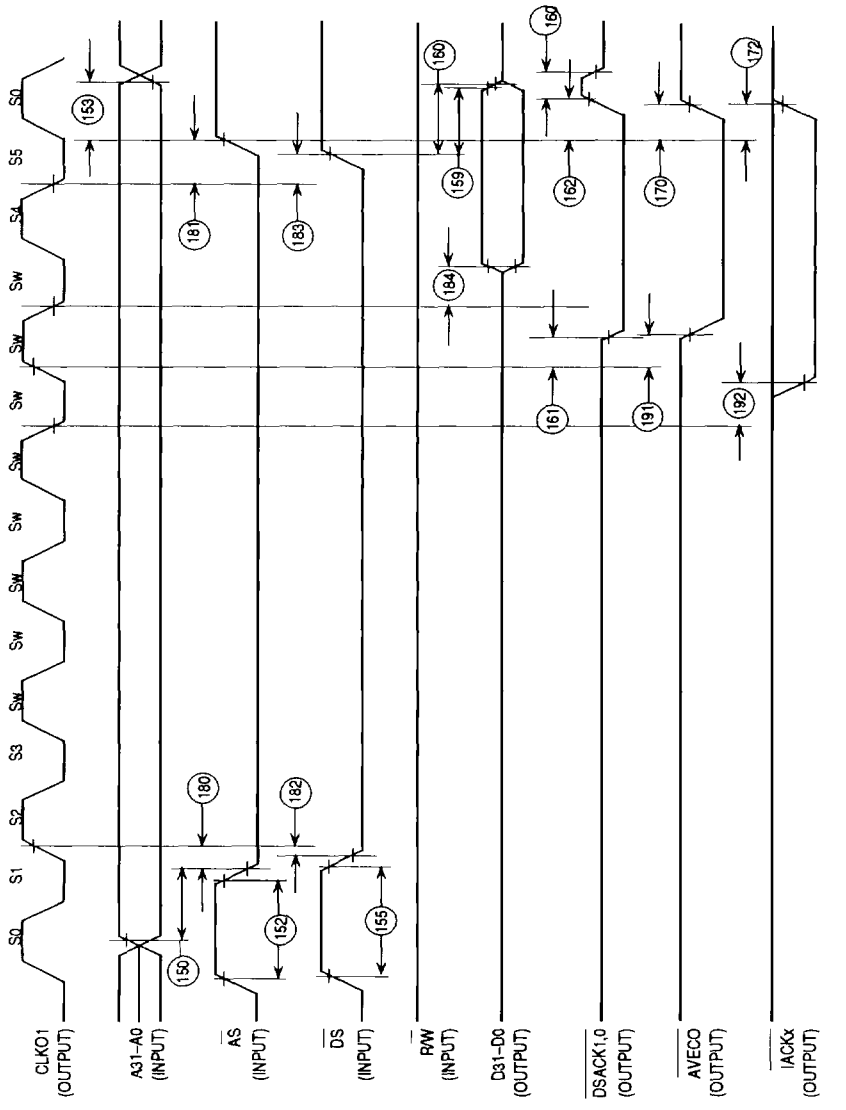


Figure 10-32. External MC68030/MC68360 Synchronous IACK Cycle Timing Diagram

10.14 030/QUICC BUS TYPE SRAM/DRAM CYCLES AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-33–Figure 10-37)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
200	$\overline{AS}$ Low to $\overline{OE}$ Low (Read Cycle)	—	20	—	15	ns
201	$\overline{AS}$ High to $\overline{OE}$ High	—	20	—	15	ns
202	$\overline{AS}$ Low to $\overline{WE}$ Low (Write Cycle)	—	20	—	15	ns
203	$\overline{AS}$ High to $\overline{WE}$ High	—	20	—	15	ns
204	CLKO1 High to $\overline{DSACK}$ High	—	20	—	15	ns
205	$\overline{AS}$ Low to $\overline{CSx}$ Low	—	22	—		ns
206	$\overline{AS}$ High to $\overline{CSx}$ High	—	20	—	15	ns
207	$\overline{AS}$ Low to $\overline{DSACK}$ Low	—	27	—	22	ns
208	$\overline{AS}$ High to $\overline{CASx}$ High	—	20	—	15	ns
210	$\overline{AS}$ Low to $\overline{BKPTO}$ Low	—	25	—	23	ns
211	$\overline{AS}$ High to $\overline{BKPTO}$ High	—	30	—	25	ns
212	Data Valid to PRTY3–0 Valid	—	20	—	15	ns
213	Data Invalid to PRTY3–0 Invalid	5	—	3.75	—	ns
214	R/$\overline{W}$ valid to $\overline{AS}$ Low	0	—	0	—	ns
215	$\overline{AS}$ High to R/$\overline{W}$ Invalid	0	—	0	—	ns
216	$\overline{AS}$ Assert to Parity Driven	4	—	3	—	ns
217	$\overline{AS}$ Negate to Parity Invalid	4	20	—	15	ns

NOTES:
1Synchronous specifications above are valid only when BSTM=1.

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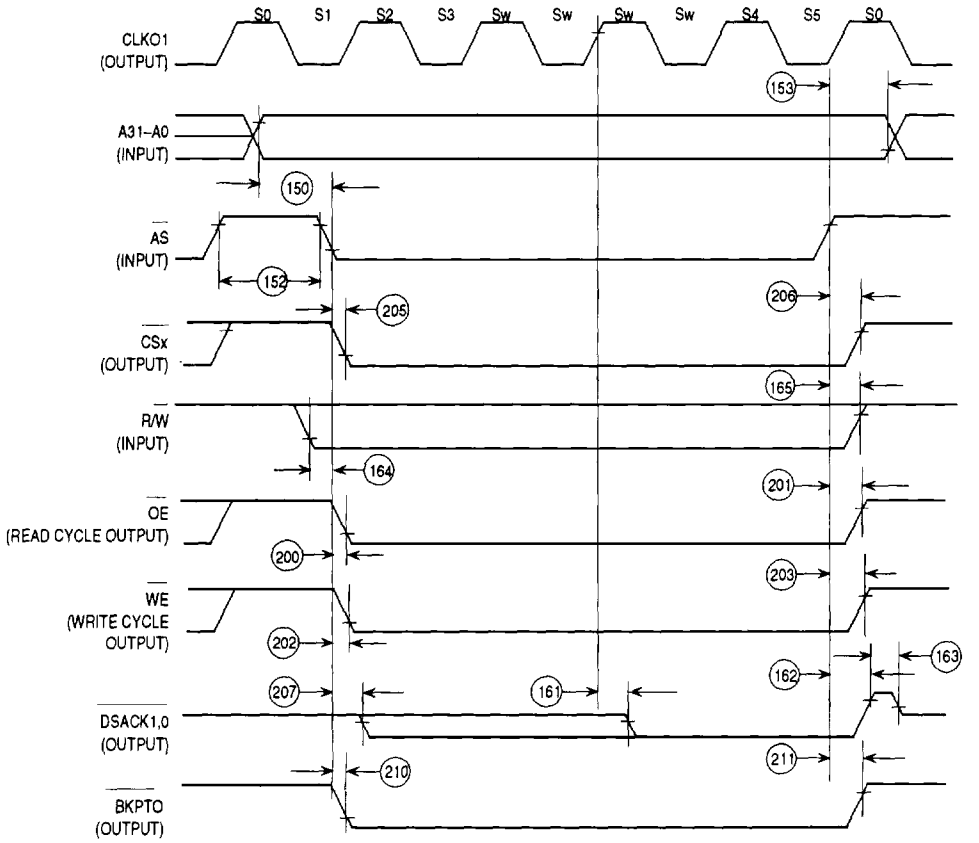

Figure 10-33. External MC68030/MC68360 SRAM Asynchronous Cycle Timing Diagram (BSTN = 0/1; SYNC = 0)

10

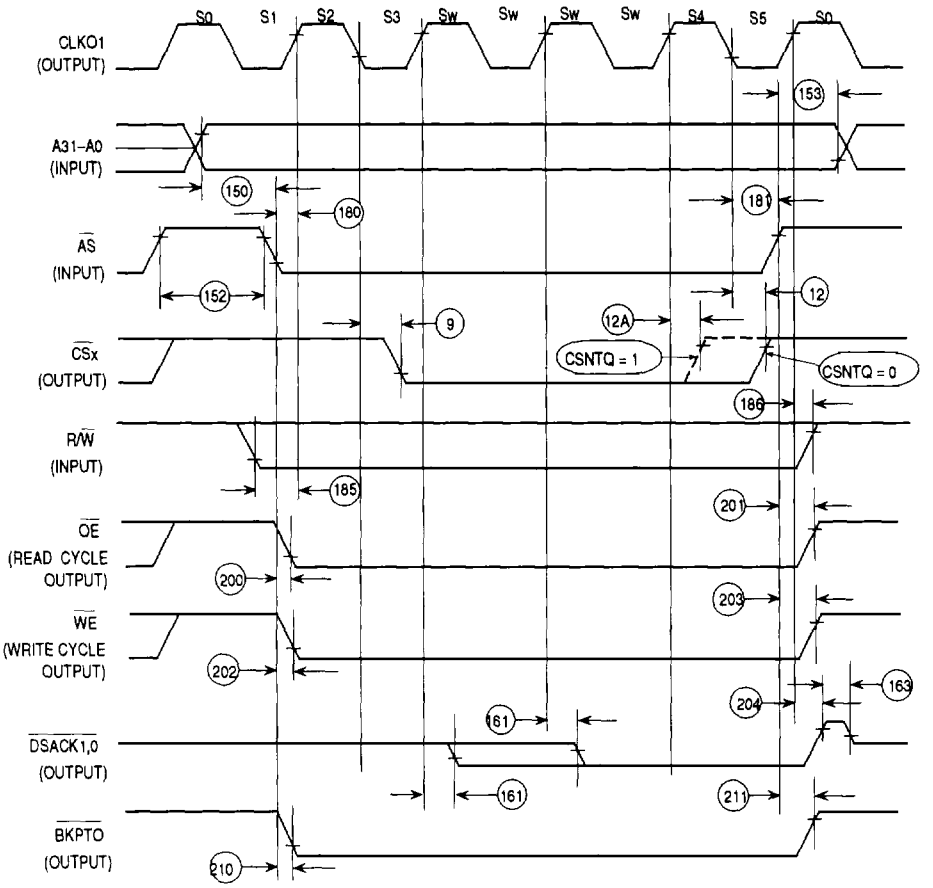

Figure 10-34. External MC68030/MC68360 SRAM Synchronous Cycle Timing Diagram (BSTM = 1; SYNC = 1)

10

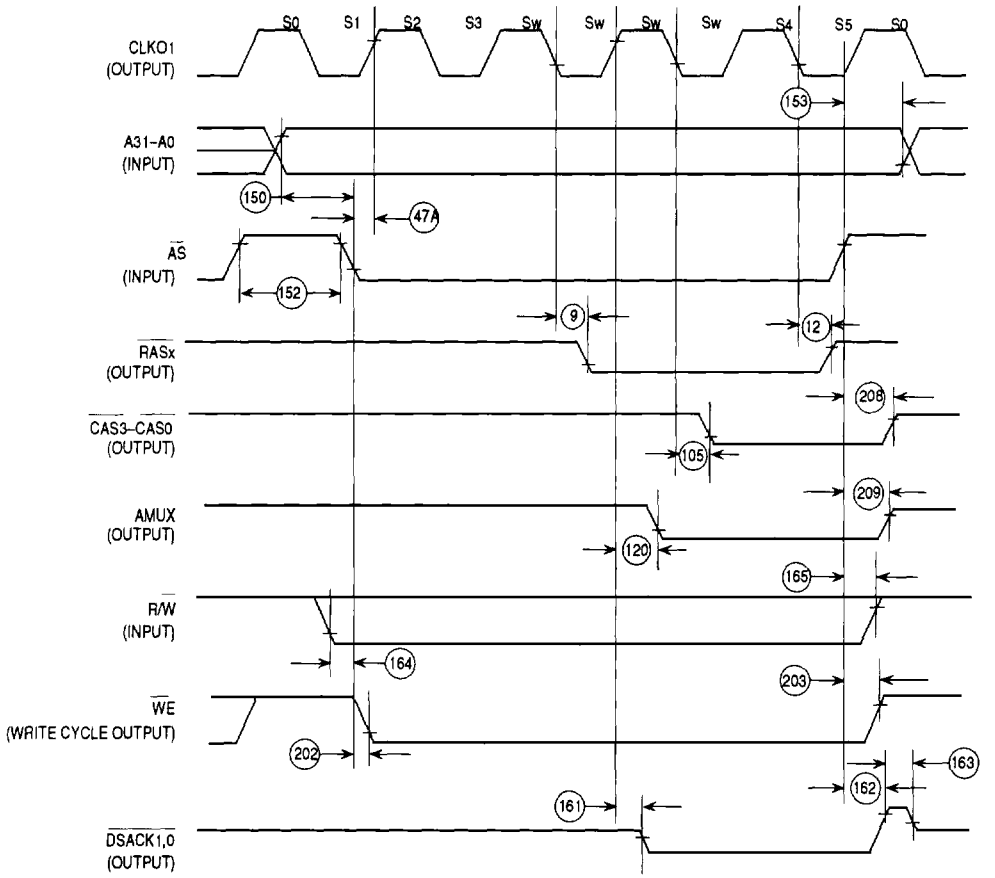

Figure 10-35. External MC68030/MC68360 DRAM Asynchronous Cycle Timing Diagram (BSTM = 0; SYNC = 0)

10

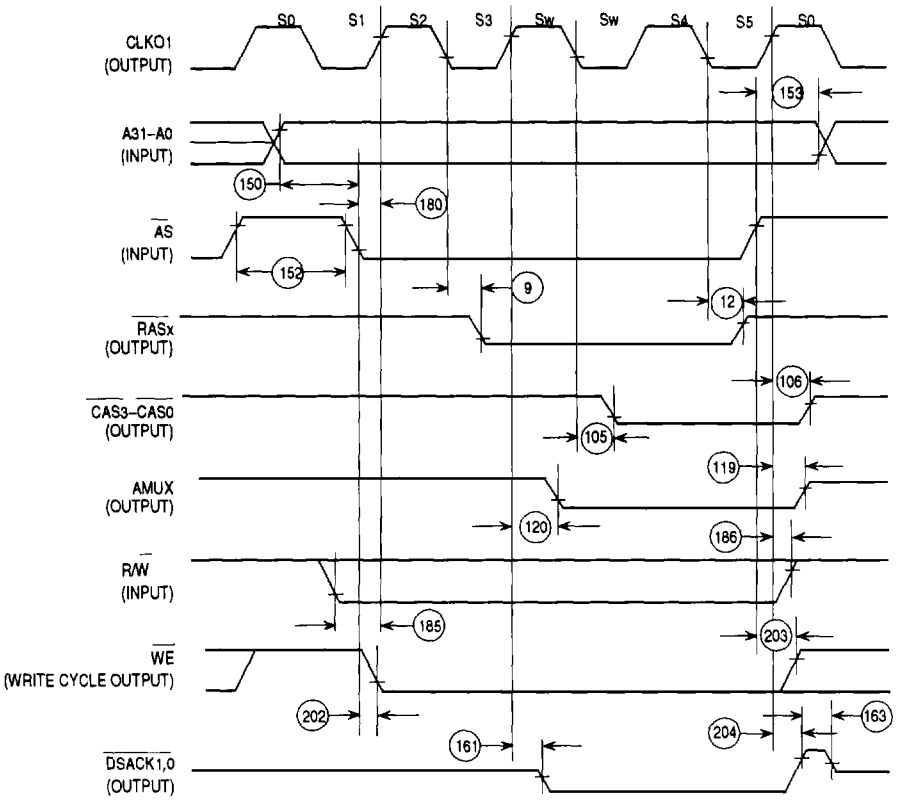

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Figure 10-36. External MC68030/MC68360 DRAM Synchronous Cycle Timing Diagram (BSTM = 1; SYNC = 1)

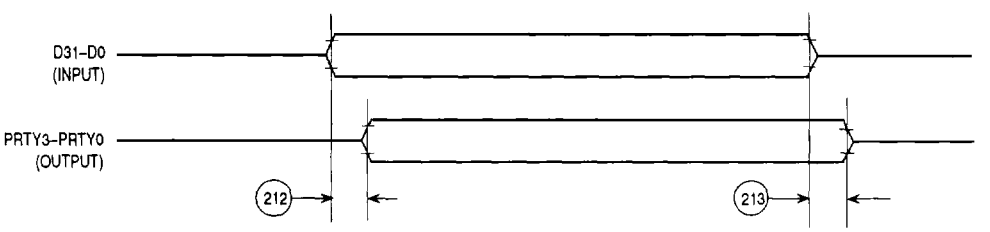

Figure 10-37. External MC68030/MC68360 Parity Bits Timing Diagram

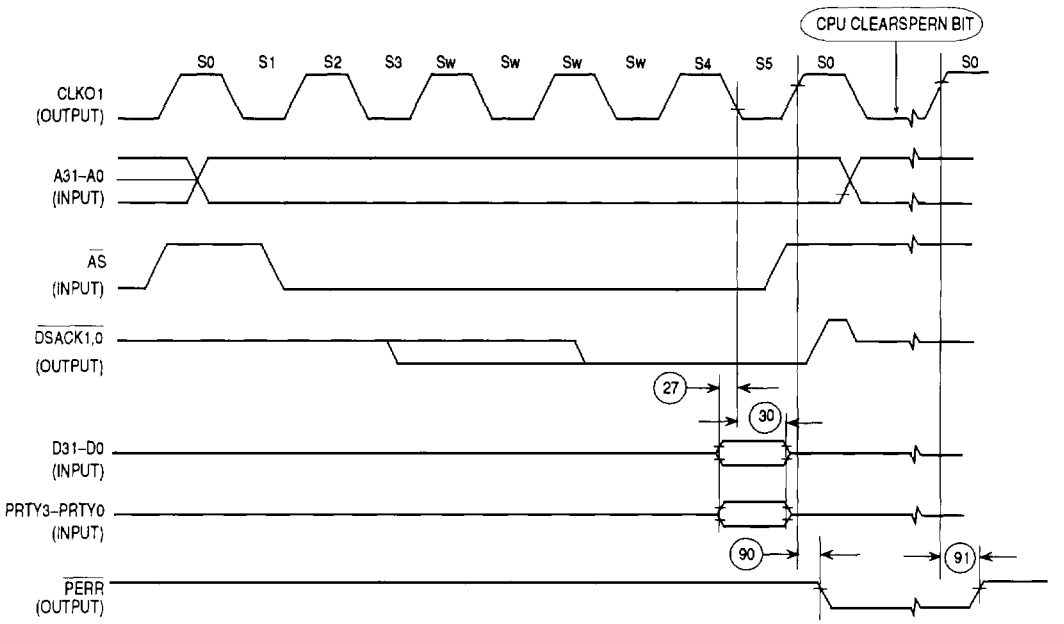

Figure 10-38. External MC68030/MC68360 Parity Bits Timing Diagram

10.15 040 BUS TYPE SLAVE MODE BUS ARBITRATION AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-39)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
231	Address, Transfer Attributes High Impedance to Clock High	7	—	6	—	ns
232[1]	Clock High to $\overline{BG}$ Low	—	20	—	15	ns
233	Clock High to $\overline{BG}$ High	4	20	4	15	ns
234	$\overline{BB}$ High to Clock High (040 output)	7	—	6	—	ns
235	$\overline{BB}$ High Impedance to Clock High (040 output)	0	—	0	—	ns
236	Clock High to $\overline{BB}$ Low (360 output)	—	20	—	15	ns
237	Clock High to $\overline{BB}$ High (360 output)	—	20	—	15	ns
238	Clock Low to $\overline{BB}$ High Impedance (360 output)	—	20	—	15	ns

NOTES:
1. $\overline{BG}$ remains low until either the SDMA or the IDMA requests the external bus.

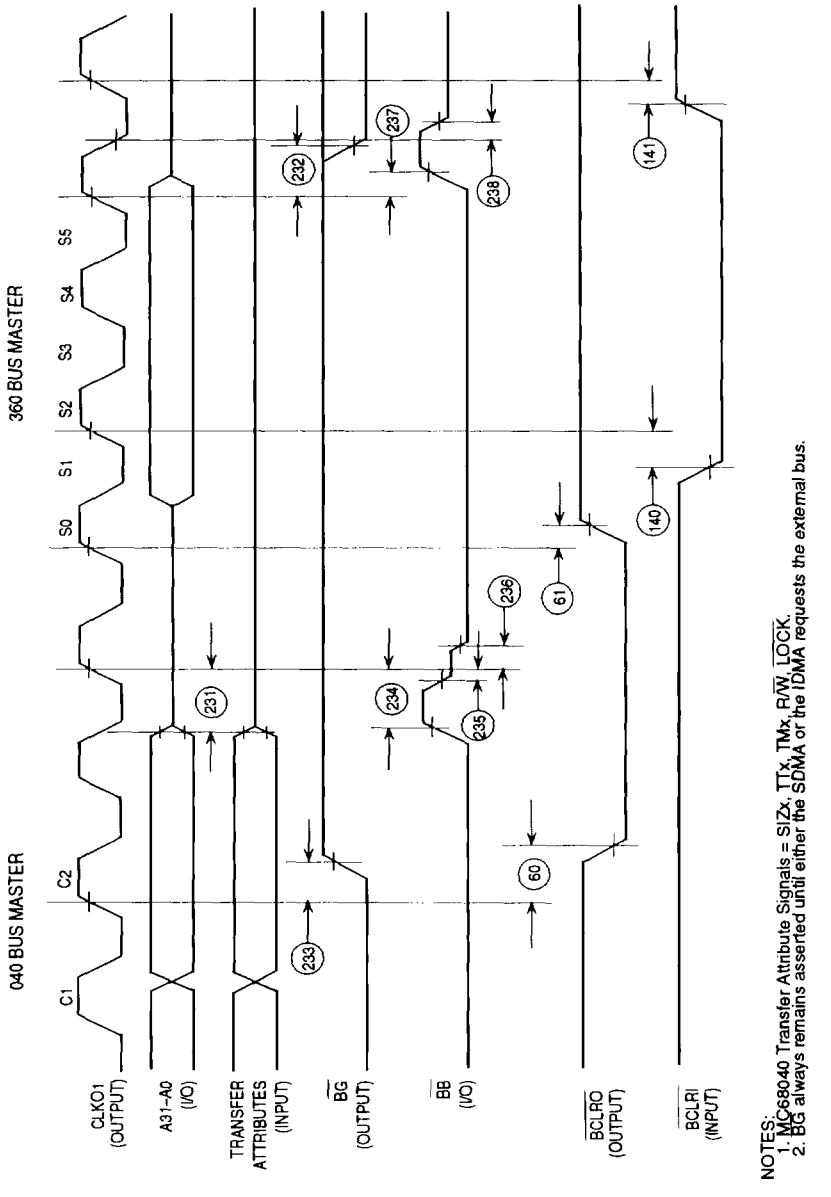

Figure 10-39. MC68040 Companion Mode Arbitration

10.16 040 BUS TYPE SLAVE MODE INTERNAL READ/WRITE/IACK CYCLES AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-40–Figure 10-42)

Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
251[1]	Address, Transfer Attributes Valid to Clock Low	15	—	11.25	—	ns
252	$\overline{TS}$ Low to Clock High	7	—	6	—	ns
253	Clock High to $\overline{TS}$ High	5	—	3	—	ns
254	Clock High to Address, Transfer Attributes Invalid	0	—	0	—	ns
255	Data-In, $\overline{MBARE}$ Valid to Clock High (040 Write)	0	—	0	—	ns
256	Clock High to Data-In, $\overline{MBARE}$ Hold Time	0	—	0	—	ns
257	Clock High to $\overline{TA}$, $\overline{TBI}$ Low (External to External)	4	20	4	15	ns
257	Clock High to $\overline{TA}$, $\overline{TBI}$ Low (External to Internal)	4	23	4	18	ns
258[2]	Clock High to $\overline{TA}$, $\overline{TBI}$ High	4	20	4	15	ns
259	$\overline{TA}$, $\overline{TBI}$ High to $\overline{TA}$, $\overline{TBI}$ High Impedance	—	15	—	11.25	ns
260	Clock Low to Data-Out Valid (040 Read)	—	20	—	15	ns
262	Clock Low to Data-Out Invalid	—	20	—	15	ns
263	Clock Low to Data-Out High Impedance	—	15	—		ns
264	Clock High to $\overline{AVECO}$ Low	—	20	—	15	ns
265	Clock Lowto $\overline{AVECO}$ High Impedance	—	30	—	23	ns
266	Clock Low to $\overline{IACK}$ Low	—	30	—	23	ns
267	Clock High to $\overline{IACK}$ High	—	30	—	23	ns
268	Clock Low to $\overline{AVEC}$ Low	—	30	—	23	ns

NOTES:
1.Transfer attributes signals = SIZx, TTx, TMx, R/W, and LOCK.
2.When MC68040 is accessing the internal registers, specification 258 is from clock low not clock high.

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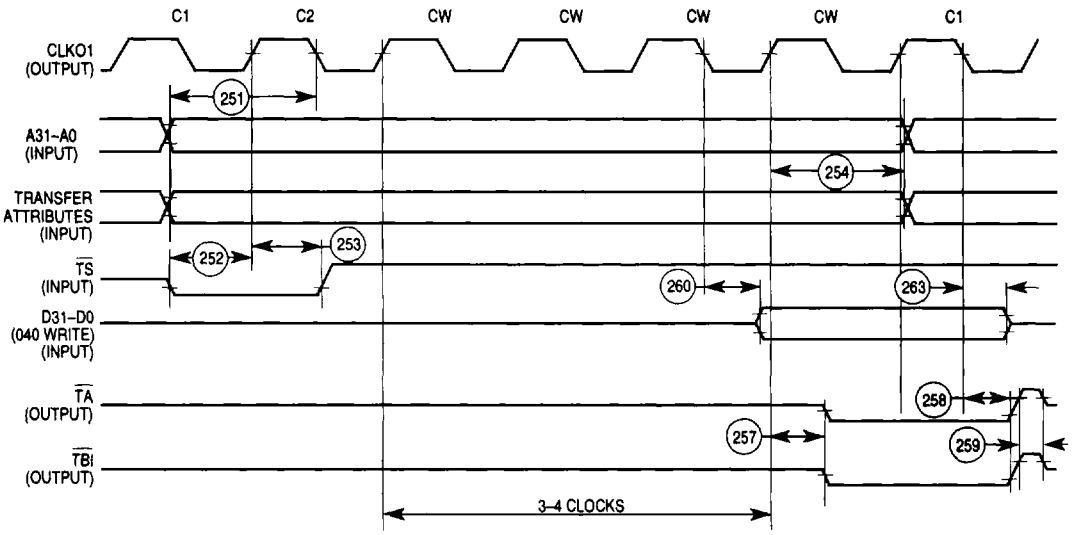

NOTES:

1. Three wait states are inserted when reading the SIM, dual-port RAM, and the CPM. Four wait states are inserted when reading the SI RAM. Additional wait states may be inserted when the SHEN1-SHEN0=10 and one of the internal masters is accessing an internal peripheral.
2. MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK

Figure 10-40. MC68040 Internal Registers Read Cycles

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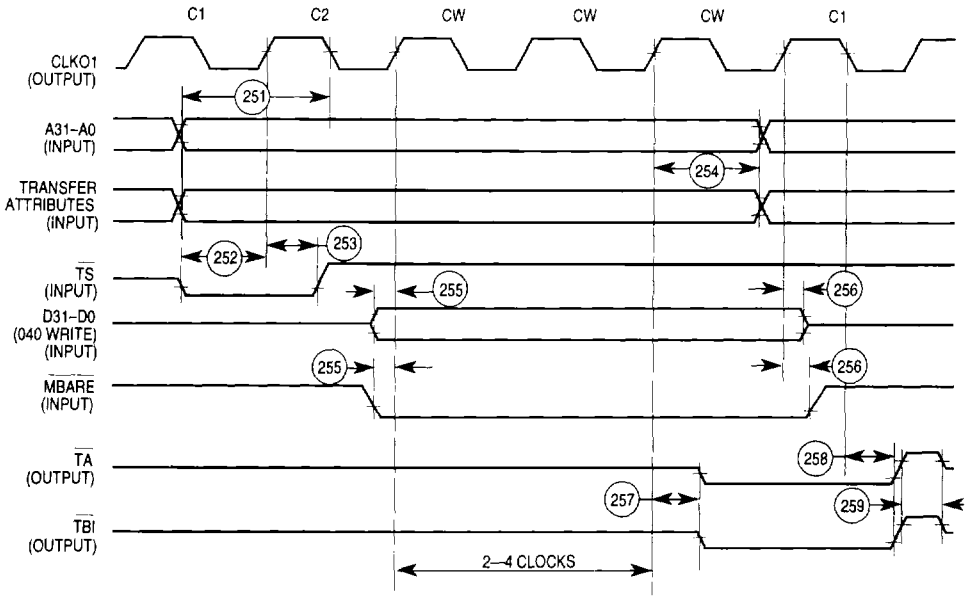
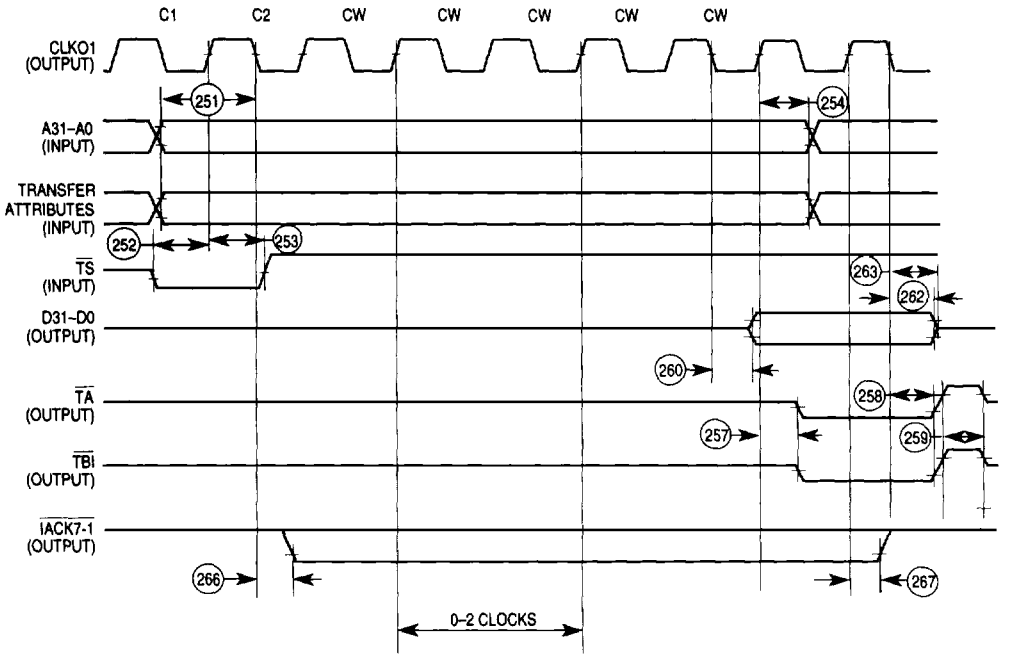


NOTES:

1. Two wait states are inserted when writing to the SIM. Three wait states are inserted when writing to the dual-port RAM and CPM. Four wait states are inserted when writing to the SI RAM. Additional wait states may be inserted when the SHEN1— SHEN0=10 and one of the internal masters is accessing an internal peripheral.
2. MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/$\overline{W}$, $\overline{LOCK}$

Figure 10-41. MC68040 Internal Registers Write Cycles

10



NOTES:
1. MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.
2. Up to two wait states may be inserted for internal arbitration.

Figure 10-42. MC68040 IACK Cycles (Vector Driven)

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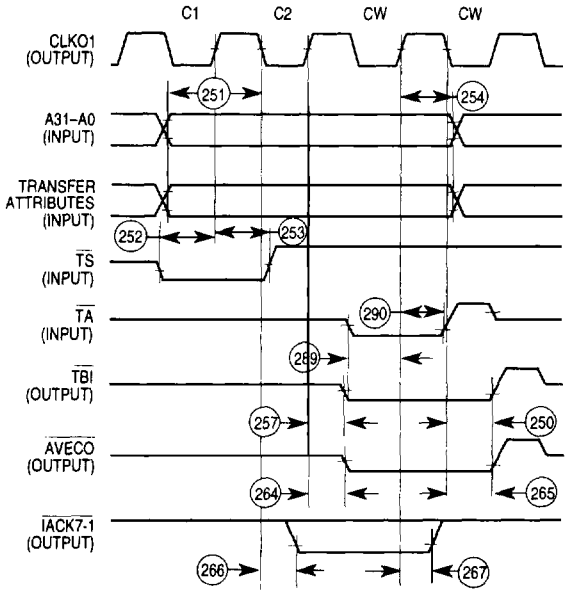

NOTES:

1. MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK.

Figure 10-43. MC68040 IACK Cycles (No Vector Driven)

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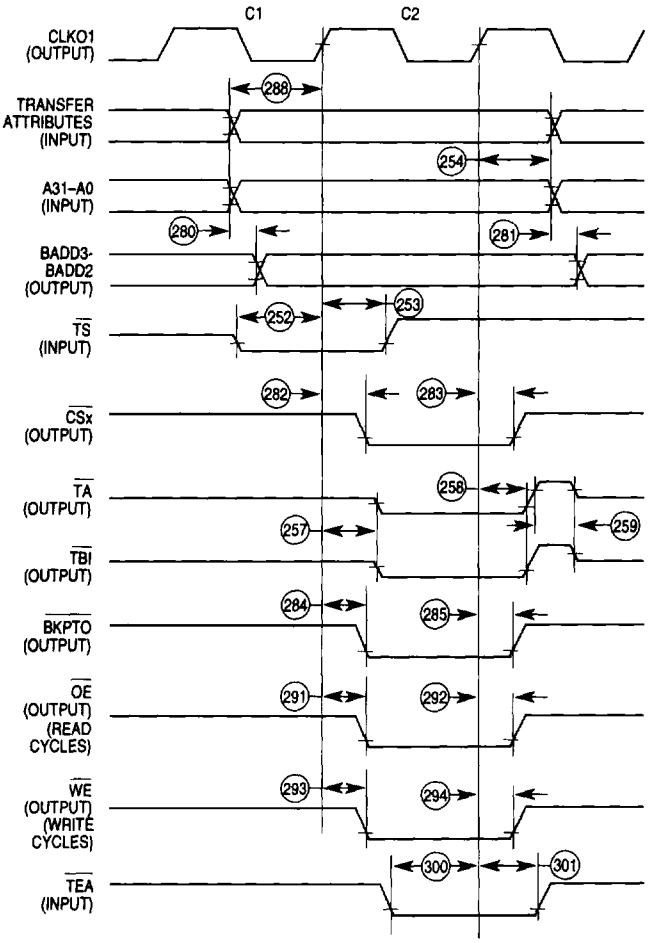
10.17 040 BUS TYPE SRAM/DRAM CYCLES AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-44–Figure 10-48)

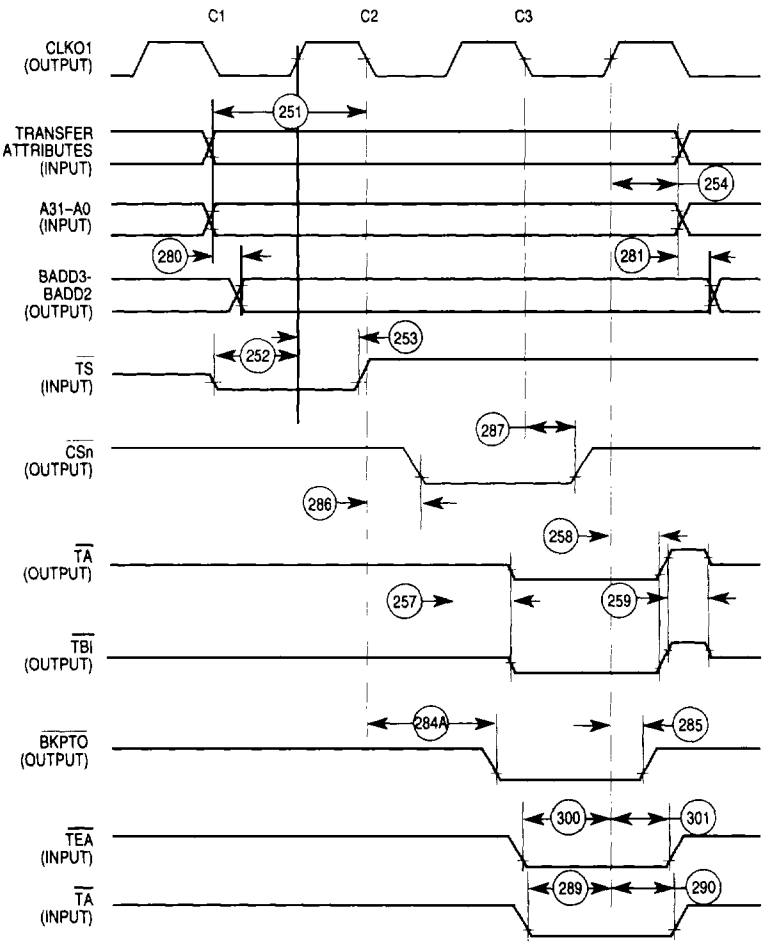
Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
280	Address Valid to BADD2–3 Valid	—	20	—	15	ns
280A	BADD2–3 Valid to CAS assertion	15	—	10	—	ns
281	Address Invalid to BADD2–3 Invalid	0	—	0	—	ns
282	Clock High to $\overline{CSx}$/$\overline{RASx}$ Low (TSS40=0)	4	16	4	12	ns
283	Clock High to $\overline{CSx}$/$\overline{RASx}$ High (CSNT40=0)	4	16	4	12	ns
284	Clock High to BRK Low	—	20	—	15	ns
284A	Clock Low to BRK Low	—	20	—	15	ns
285	Clock High to BRK High	—	20	—	15	ns
286	Clock Low to $\overline{CSx}$ /$\overline{RASx}$ Low (TSS40=1)	4	16	4	12	ns
287	Clock Low to $\overline{CSx}$ /$\overline{RASx}$ High (CSNT40=1)	4	16	4	12	ns
288[1]	AddressTransfer Attributes Valid to Clock High (TSS40=0)	12	—	11	—	ns
289[2]	$\overline{TA}$ Low to Clock High (External Termination)	11	—	9	—	ns
290[2]	Clock High to $\overline{TA}$ High (External Termination)	—	20	—	15	ns
291	Clock High to $\overline{OE}$ Low (Read Cycles)	—	20	—	15	ns
292	Clock High to $\overline{OE}$ High (Read Cycles)	—	20	—	15	ns
293	Clock High to $\overline{WE}$ Low (Write Cycles)	—	20	—	15	ns
294	Clock High to $\overline{WE}$ High (Write Cycles)	—	20	—	15	ns
295	Clock High to $\overline{CASx}$ Low	4	13	4	10	ns
295A	Clock High to $\overline{CASx}$ High (040 Burst Read only)	4	13	4	10	ns
296	Clock High to $\overline{CASx}$ High	4	13	4	10	ns
297	Clock Low to AMUX Low	3	16	3	12	ns
298	Clock High to AMUX High	3	16	3	12	ns
299	Clock High to BADD2–3 Valid (040 Burst Cycles)	4	20	4	15	ns
300[2]	$\overline{TEA}$ Low to Clock High	11	—		—	ns
301[2]	Clock High to $\overline{TEA}$ High	2	20	2	15	ns
302	Data, Parity Valid to Clock High (Data, Parity Set-up)	7	—	6	—	ns
303	Clock High to Data, Parity Invalid (Data, Parity Hold)	7	—	5	—	ns
305	CLKO1 High (After $\overline{TS}$ low) to Parity Valid	—	20	—	15	ns
306	CLKO1 High (After $\overline{TA}$ low) to Parity Hi-Z	4	20		15	ns

NOTES:
1.Transfer attributes signals = SIZx, TTx, TMx, R/$\overline{W}$, and $\overline{LOCK}$.
2.TEA/$\overline{TA}$ should not be asserted on a DRAM burst access, or on the same clock or before $\overline{RASx}$ / $\overline{CSx}$ is asserted



NOTE: MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK

Figure 10-44. MC68040 SRAM Read/Write Cycles (TSS40 =0, CSNT40 = 0)



NOTE: MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK

Figure 10-45. MC68040 SRAM Read/Write Cycles (TSS40 =1, CSNT40 = 1)

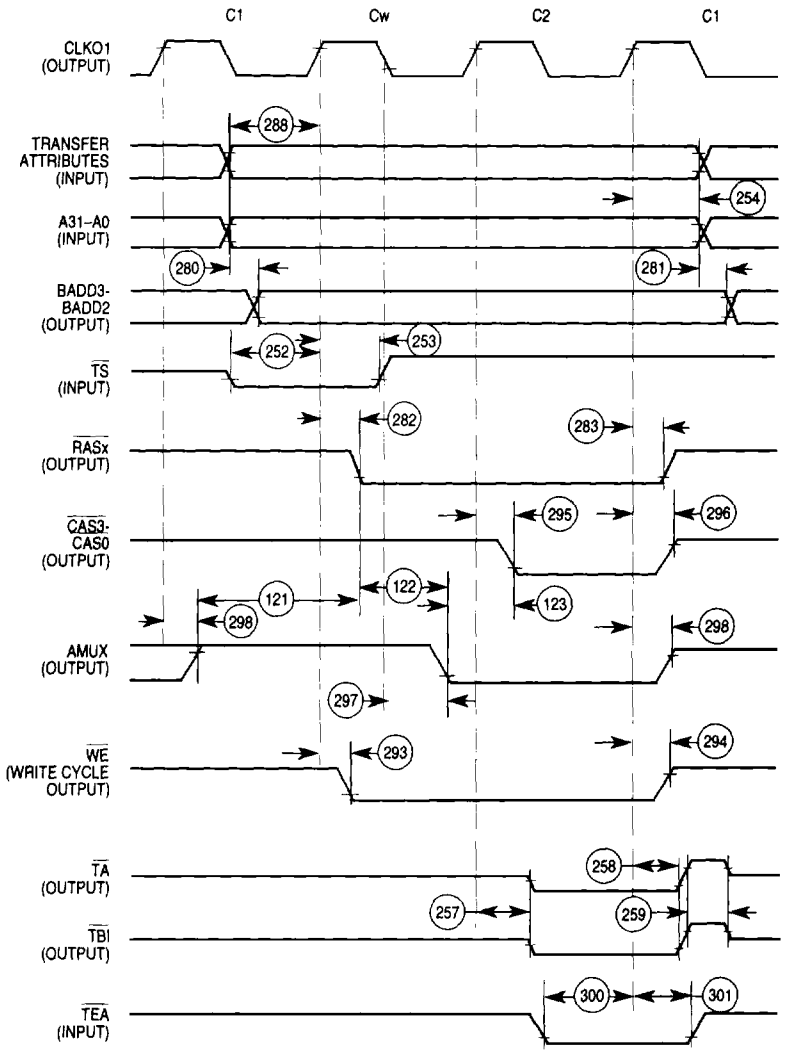


Figure 10-46. External MC68040 DRAM Cycles Timing Diagram

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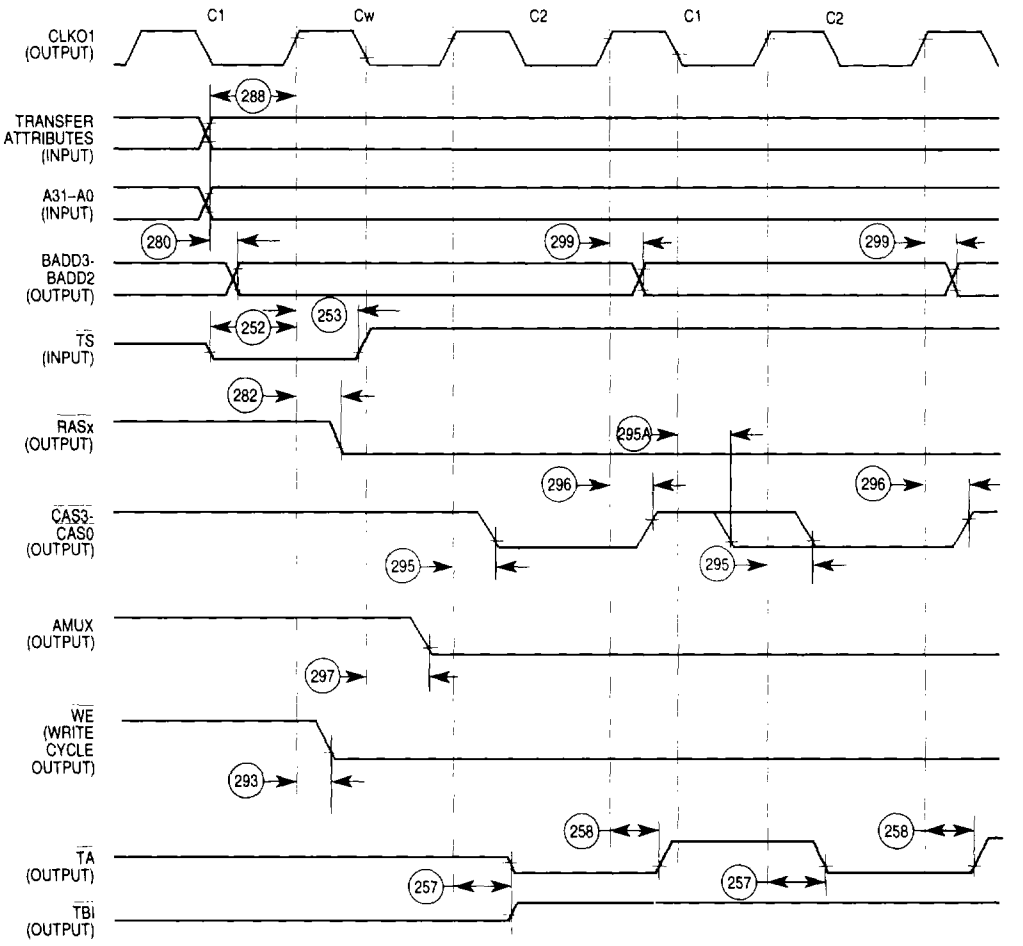

Figure 10-47. External MC68040 DRAM Burst Cycles Timing Diagram

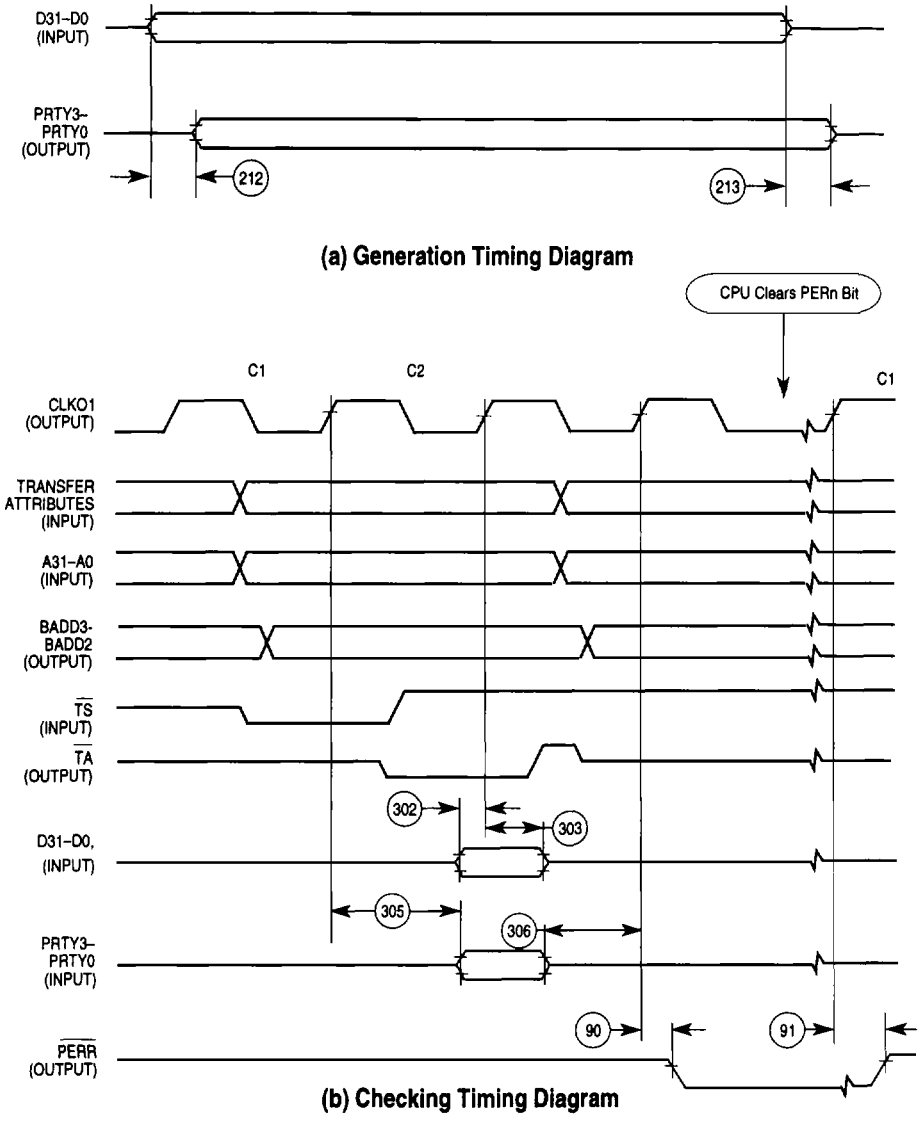

Figure 10-48. External MC68040 Parity Bit Checking Timing Diagram

10.18 IDMA AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-49 and Figure 10-50.)

Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
1	CLKO1 Low to $\overline{DACK}$, $\overline{DONE}$ Asserted	—	24	—	18	ns
2	CLKO1 Low to $\overline{DACK}$, $\overline{DONE}$ Negated	—	24	—	18	ns
3[1]	$\overline{DREQ}$x Asserted to $\overline{AS}$ Asserted (for DMA Bus Cycle)	$3t_{cyc} + t_{AIST} + t_{CLSA}$				
4[1]	Asynchronous Input Setup Time to CLKO1 Low	12	—	9	—	ns
5[1]	Asynchronous Input Hold Time from CLKO1 Low	0	—	0	—	ns
6	$\overline{AS}$ to $\overline{DACK}$ Assertion Skew	0	20	0	15	ns
7	$\overline{DACK}$ to $\overline{DONE}$ Assertion Skew	-8	8	-6	6	ns
8	$\overline{AS}$, $\overline{DACK}$, $\overline{DONE}$ Width Asserted	70	—	52.5	—	ns
8A	$\overline{AS}$, $\overline{DACK}$, $\overline{DONE}$ Width Asserted (Fast Termination Cycle)	28	—	20.5	—	ns
10[1]	Asynchronous Input Setup Time to CLKO1 Low	5	—	4	—	ns
11[1]	Asynchronous Input Hold Time from CLKO1 Low	10	—	7.5	—	ns
12[2]	DREQ Input Setup Time to CLKO1 Low	20	—	15	—	ns
13[2]	DREQ Input Hold Time from CLKO1 Low	5	—	3.75	—	ns
14[2]	DONE Input Setup Time to CLKO1 Low	20	—	15	—	ns
15[2]	DONE Input Hold Time from CLKO1 Low	5	—	3.75	—	ns
16[2]	DREQ Asserted to $\overline{AS}$ Asserted	2	—	2	—	clk

NOTES:
1.These specifications are for asynchronous mode.
2.These specifications are for synchronous mode.

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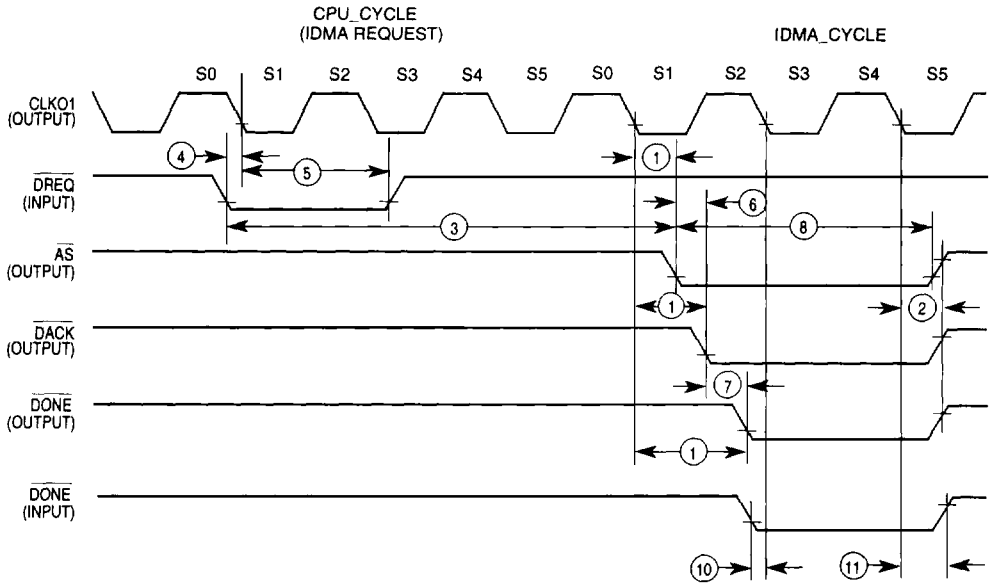


Figure 10-49. IDMA Signal Asynchronous Timing diagram

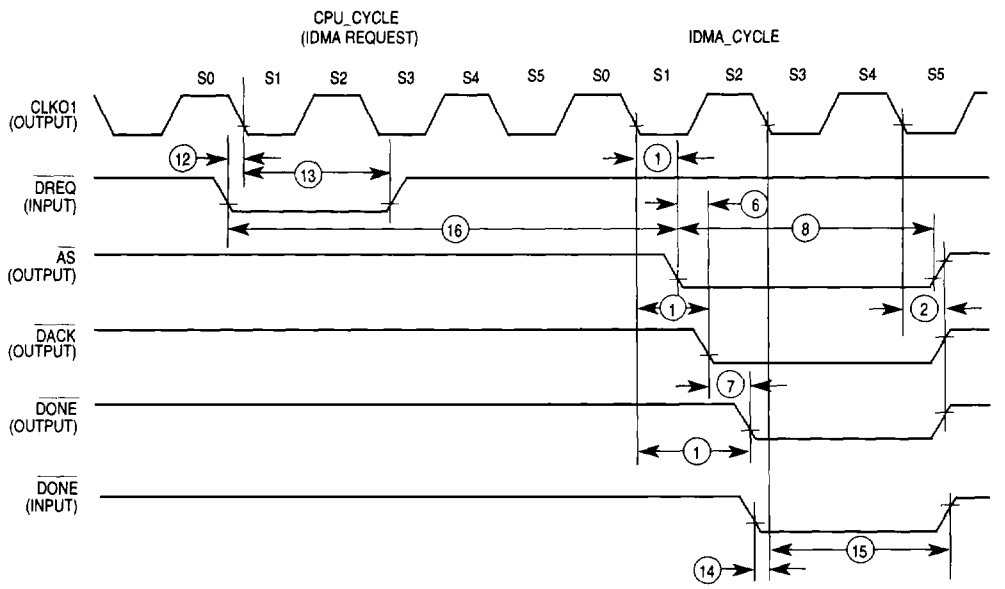


Figure 10-50. IDMA Signal Synchronous Timing diagram

10.19 PIP/PIO AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-51– Figure 10-55)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.3 MHz		Unit
		Min	Max	Min	Max	
21	Data-In Setup Time to STBI Low	0	—	0	—	ns
22	Data-In Hold Time to STBI High	2.5– t3	—	2.5– t3	—	clk
23	STBI Pulse Width	1.5	—	1.5	—	clk
24	STBO Pulse Width	1 CLKO1 - 5ns	—	1 CLKO1 - 5ns	—	-
25	Data-Out Setup Time to STBO Low	2	—	2	—	clk
26	Data-Out Hold Time from STBO High	5	—	5	—	clk
27	STBI Low to STBO Low (Rx Interlock)	—	2	—	2	clk
28	STBI Low to STBO High (Tx Interlock)	2	—	2	—	clk
29	Data-In Setup Time to Clock Low	20	—	15	—	ns
30	Data-In Hold Time from Clock Low	10	—	7.5	—	ns
	Clock High to Data-Out Valid (CPU Writes Data, Control, or Direction)	—	25	—	25	ns

Note: t3 = Spec. 3 on Table 10.7

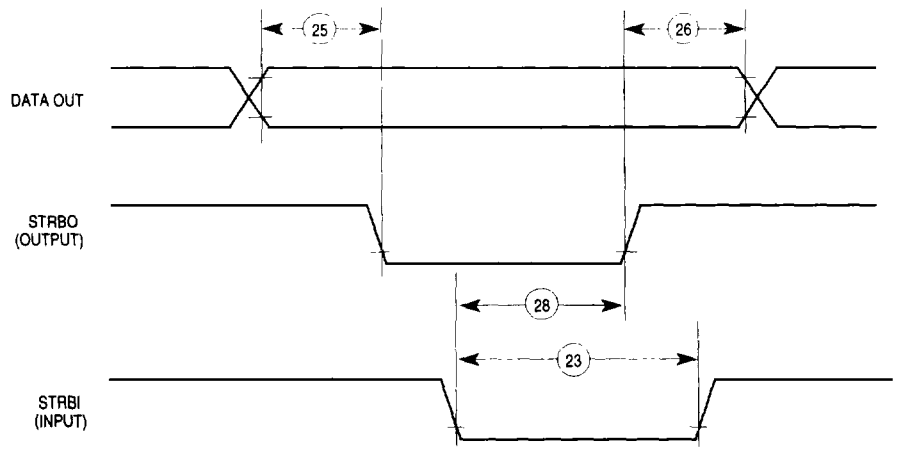


Figure 10-51. PIP Rx (Interlock Mode)

10

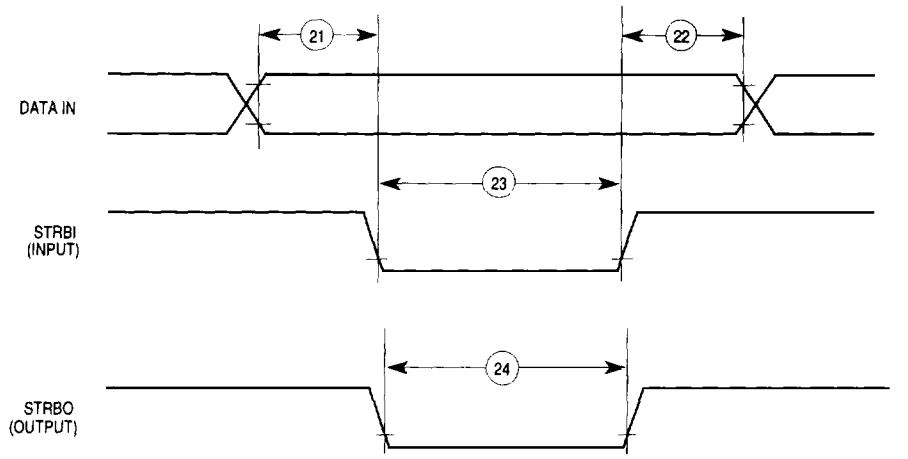


Figure 10-52. PIP Tx (Interlock Mode)

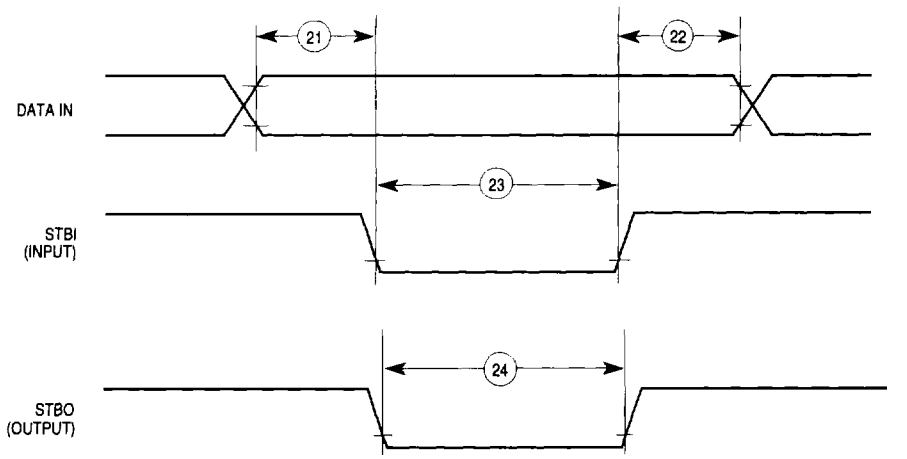


Figure 10-53. PIP Tx (Pulse Mode)

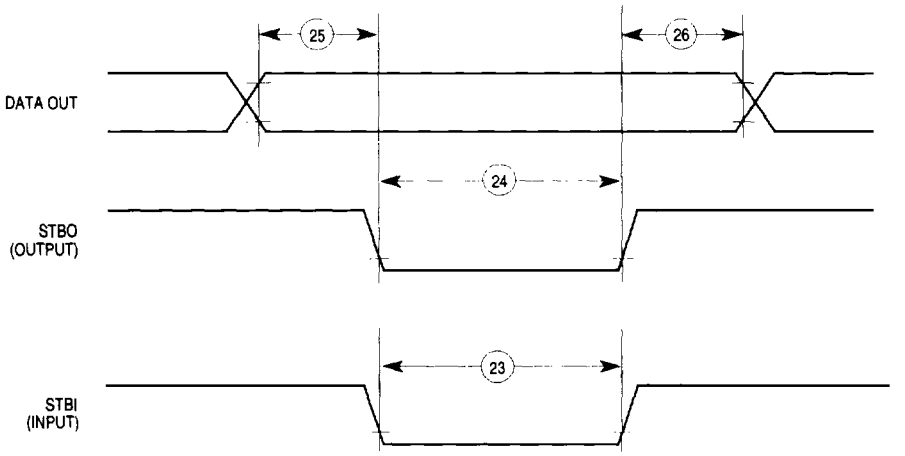


Figure 10-54. PIP Tx (Pulse Mode)

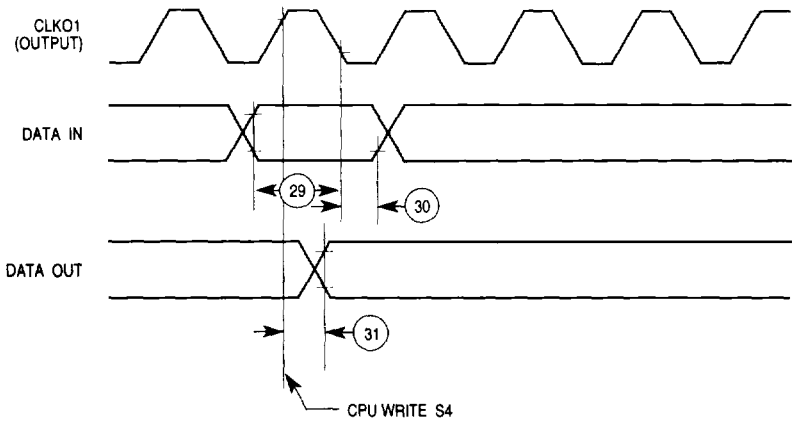


Figure 10-55. Parallel I/O Data-in/Data-Out Timing Diagram

10.20 INTERRUPT CONTROLLER AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-56 and Figure 10-57)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
35	Port C Interrupt Pulse Width Low (Edge Triggered Mode)	70	—	55	—	ns
36	Minimum Time Between Active edges PortC	70	—	55	—	clk
37	Clock High to $\overline{IOUT}$ Valid (Slave Mode)	—	20	—	17	ns
38	Clock High to $\overline{RQOUT}$ Valid (Slave Mode)	—	20	—	17	ns

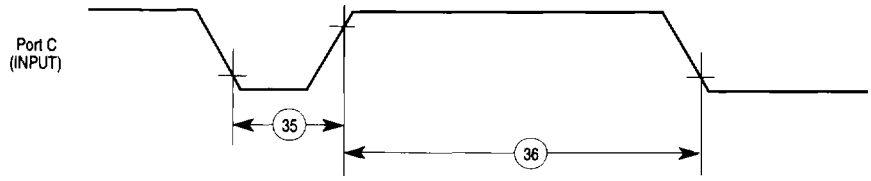


Figure 10-56. Interrupts Timing Diagram

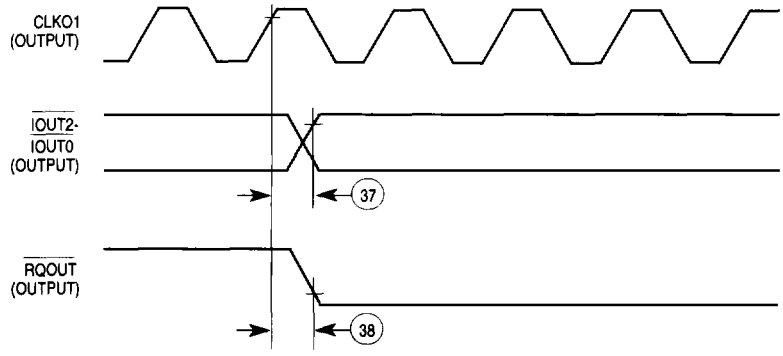


Figure 10-57. Slave Mode: Interrupts Timing Diagram

10.21 BAUD RATE GENERATOR AC ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-58)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
50	BRGO Rise and Fall Time	—	10	—	7.5	ns
51	BRGO Duty Cycle	40	60	40	60	%
52	BRGO Cycle	40		30		ns

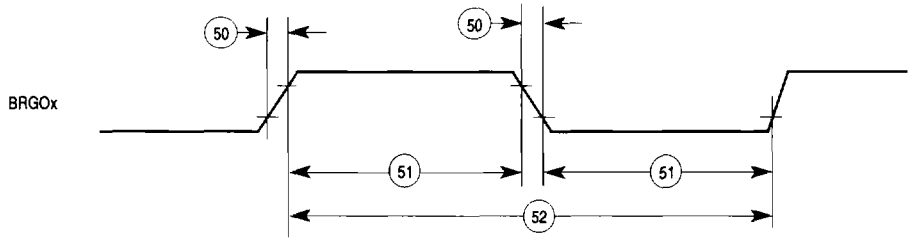


Figure 10-58. Baud Rate Generator Output Signals

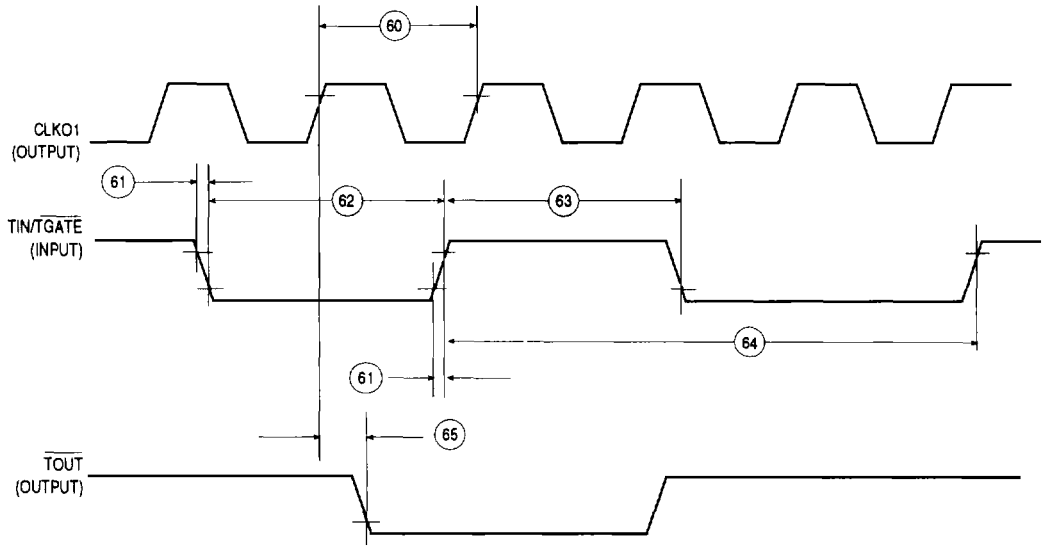


Figure 10-59. CPM General Purpose Timers

10.22 TIMER ELECTRICAL SPECIFICATIONS

The electrical specifications in this document are preliminary. See Figure 10-59)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 25 MHz		5.0 V 33.34MHz		Unit
			Min	Max	Min	Max	
61	TIN/TGATE Rise and Fall Time	t_{rf}	10	—	10	—	ns
62	TIN/TGATE Low Time	—	1	—	1	—	clk
63	TIN/TGATE High Time	—	2	—	2	—	clk
64	TIN/TGATE Cycle Time	—	3	—	3	—	clk
65	CLKO1 High to TOUT Valid	t_{TO}	3	25	3	22	ns

10.23 SI ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-60–Figure 10-64.)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
70[1,3]	L1RCLK, L1TCLK Fequency (DSC=0)	—	10	—	10	MHz
71[3]	L1RCLK, L1TCLK Width Low(DSC=0)	P+10	—	P+10	—	ns
71A[2]	L1RCLK, L1TCLK Width High (DSC=0)	P+10	—	P+10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO Rise/Fall Time	—	15	—	15	ns
73	L1RSYNC, L1TSYNC Valid to L1CLK edge (SYNC Setup Time)	20	—	20	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC Invalid (SYNC Hold Time)	35	—	35	—	ns
75	L1RSYNC, L1TSYNC Rise/Fall Time	—	15	—	15	ns
76	L1RXD Valid to L1CLK edge (L1RXD Setup Time)	42	—	42	—	ns
77	L1CLK edge to L1RXD Invalid (L1RXD Hold Time)	35	—	35	—	ns
78	L1CLK edge to L1ST(1–4) Valid	10	45	10	45	ns
78A[4]	L1SYNC Valid to L1ST(1–4) Valid	10	45	10	45	ns
79	L1CLK Edge to L1ST(1–4) Invalid	10	45	10	45	ns
80	L1CLK Edge to L1TXD Valid	10	65	10	65	ns
80A[4]	L1TSYNC Valid to L1TXD Valid	10	65	10	65	ns
81	L1CLK Edge to L1TXD High Impedance	0	42	0	42	ns
82	L1RCLK, L1TCLK Fequency (DSC=1)	—	12.5	—	16	MHz
83	L1RCLK, L1TCLK Width Low(DSC=1)	P+10	—	P+10	—	ns
83A[2]	L1RCLK, L1TCLK Width High (DSC=1)	P+10	—	P+10	—	ns
84	L1CLK Edge to L1CLKO Valid (DSC=1)	—	30	—	30	ns
85[3]	L1RQ Valid Before Falling Edge of L1TSYNC	1	—	1	—	L1TCLK
86[3]	L1GR Setup Time	42	—	42	—	ns
87[3]	L1GR Hold Time	42	—	42	—	ns
88	L1CLK edge to L1SYNC Valid (FSD = 00, CNT = 0000, BYT = 0, DSC=0)	—	0	—	0	ns

NOTES:
1. The ratio SyncCLK/L1RCLK must be greater than 2.5/1
2. Where P=1/CLKO1. Thus for a 25 MHz CLKO1 rate, P=40ns.
3. These specs are valid for IDL mode only
4. The strobes and Txd on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

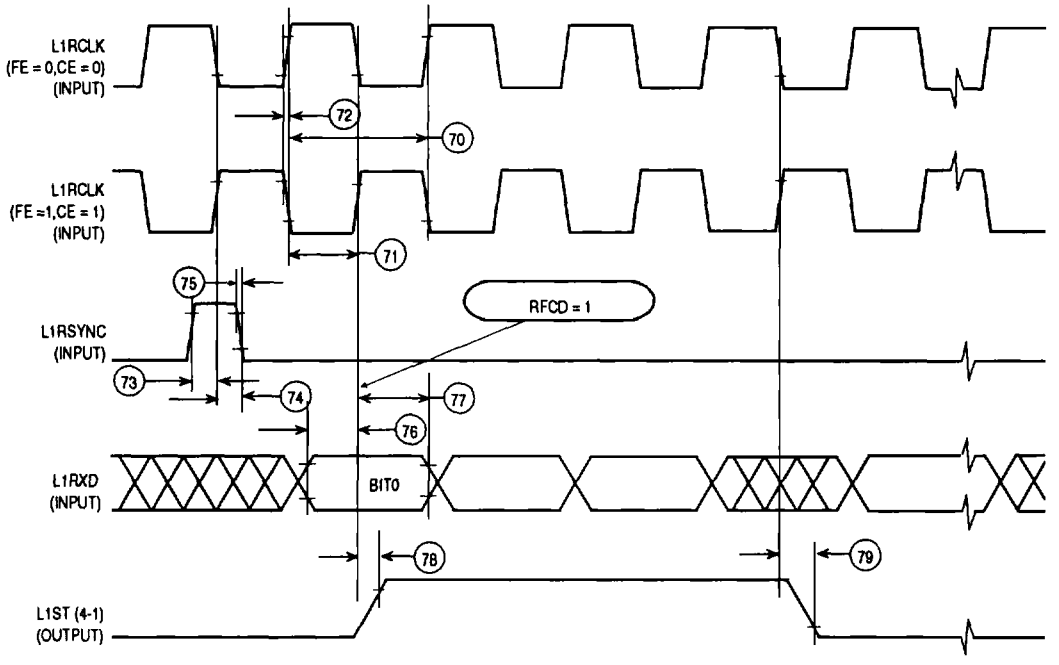


Figure 10-60. SI Receive Timing with Normal Clocking (DSC = 0)

10

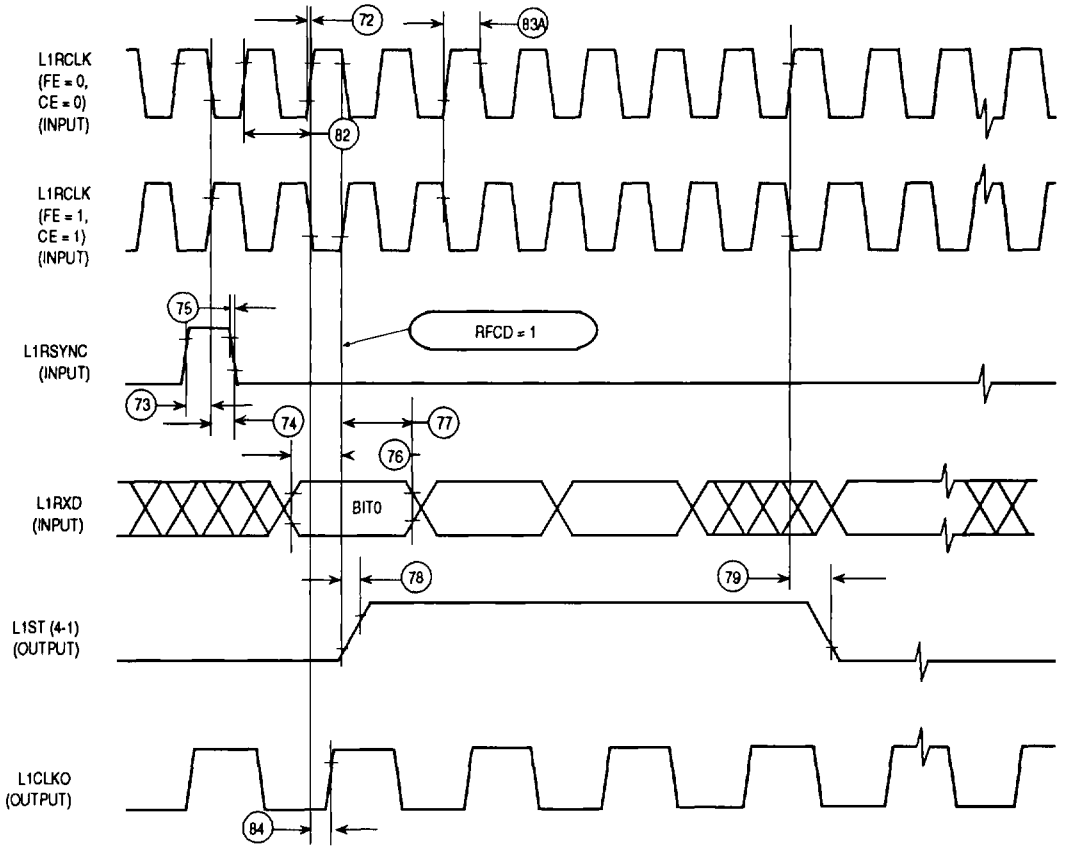


Figure 10-61. SI Receive Timing with Double Speed Clocking (DSC = 1)

10

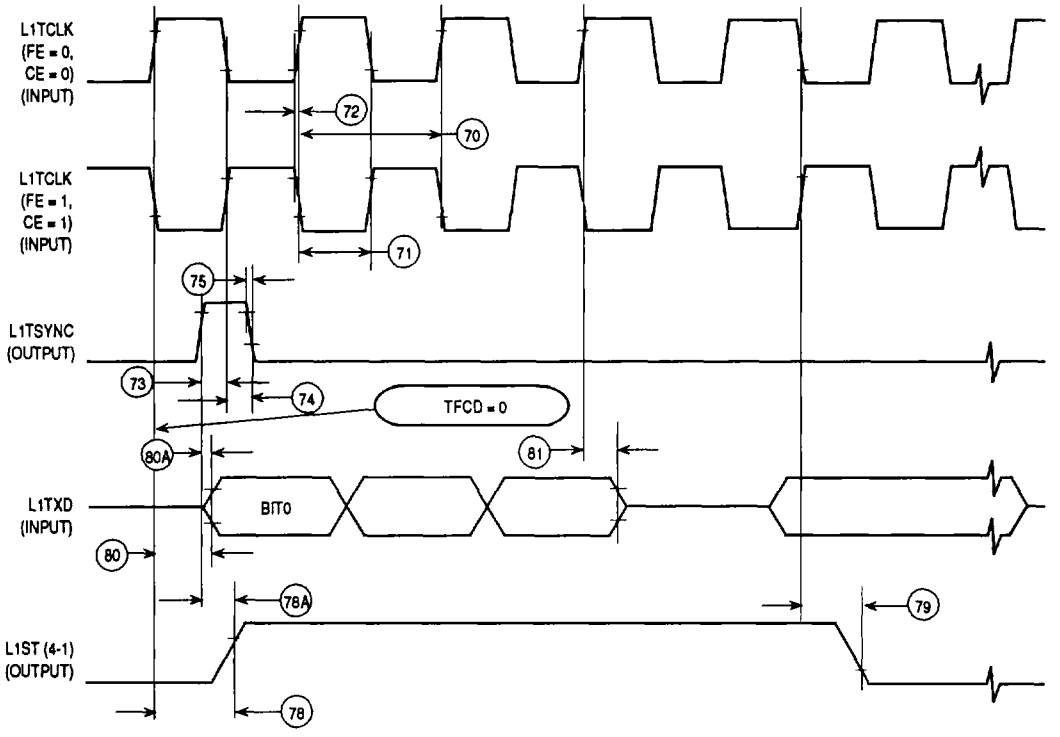


Figure 10-62. SI Transmit Timing with Normal Clocking (DSC = 0)

10

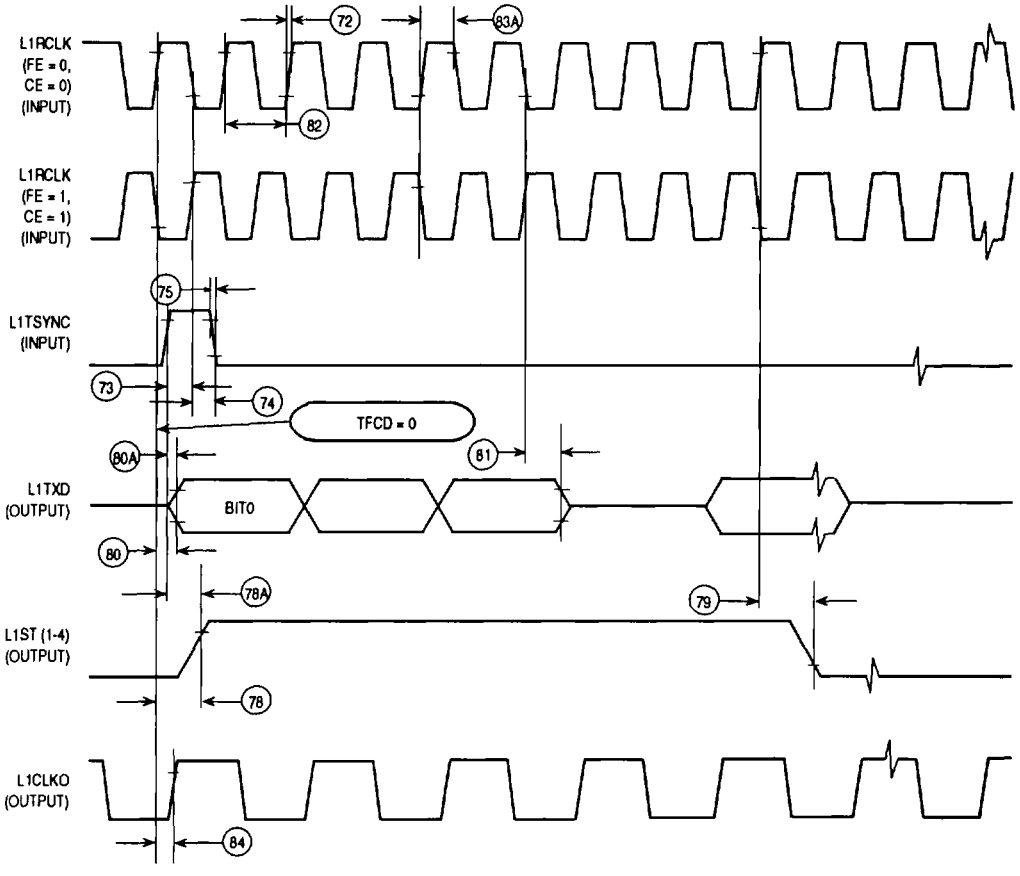


Figure 10-63. SI Transmit Timing with Double Speed Clocking (DSC = 1)

10

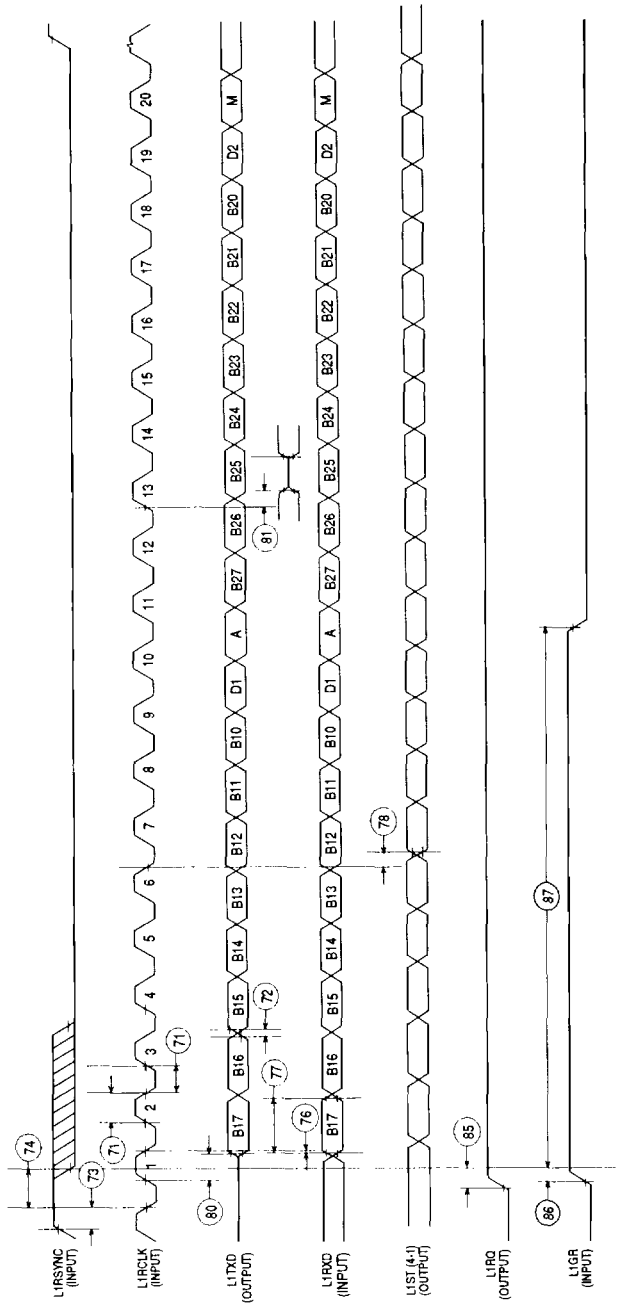


Figure 10-64. IDL Timing

10.24 SCC IN NMSI MODE—EXTERNAL CLOCK ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-65–Figure 10-67)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
100[1]	RCLK1 and TCLK1 Width High	CLKO1	—	CLKO1	—	
101	RCLK1 and TCLK1 Width Low	CLKO1 + 5nS	—	CLKO1 + 5nS	—	
102	RCLK1 and TCLK1 Rise/Fall Time	—	15	—	15	ns
103	TXD1 Active Delay (From TCLK1 Falling Edge)	0	50	0	50	ns
104	$\overline{\text{RTS1}}$ Active/Inactive Delay (From TCLK1 Falling Edge)	0	50	0	50	ns
105	$\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge	5	—	5	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	5	—	5	—	ns
107[2]	RXD1 Hold Time from RCLK1 Rising Edge	5	—	5	—	ns
108	$\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge	5	—	5	—	ns

NOTES:
1.The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1
2.Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

10.25 SCC IN NMSI MODE—INTERNAL CLOCK ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-65–Figure 10-67)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
100[1]	RCLK1 and TCLK1 Frequency	0	8.3	0	11	MHz
102	RCLK1 and TCLK1 Rise/Fall Time	—	—	—	—	ns
103	TXD1 Active Delay (From TCLK1 Falling Edge)	0	30	0	30	ns
104	$\overline{\text{RTS1}}$ Active/Inactive Delay (From TCLK1 Falling Edge)	0	30	40	—	ns
105	$\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge	40	—	40	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	40	—	0	—	ns
107[2]	RXD1 Hold Time from RCLK1 Rising Edge	0	—	40	—	ns
108	$\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge	40	—	0	30	ns

NOTES:
1.The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1
2.Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

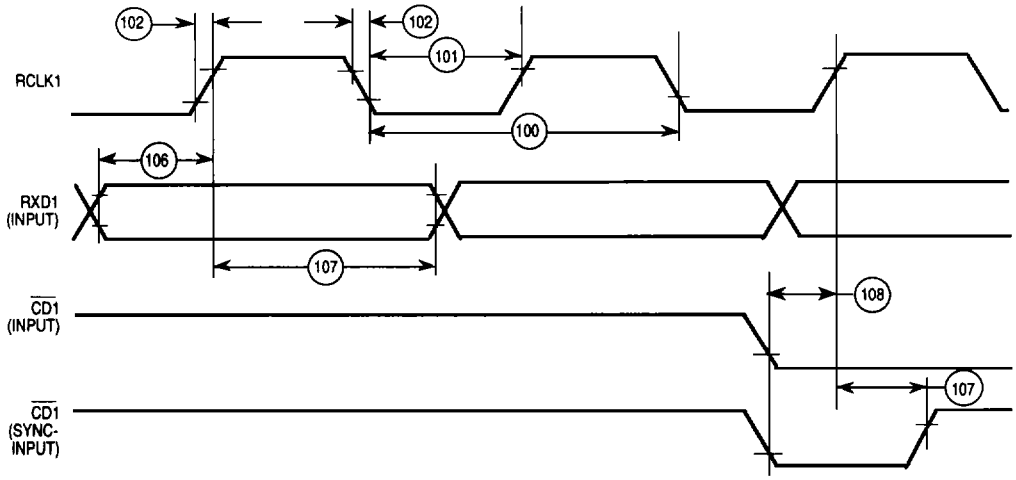


Figure 10-65. SCC NMSI Receive

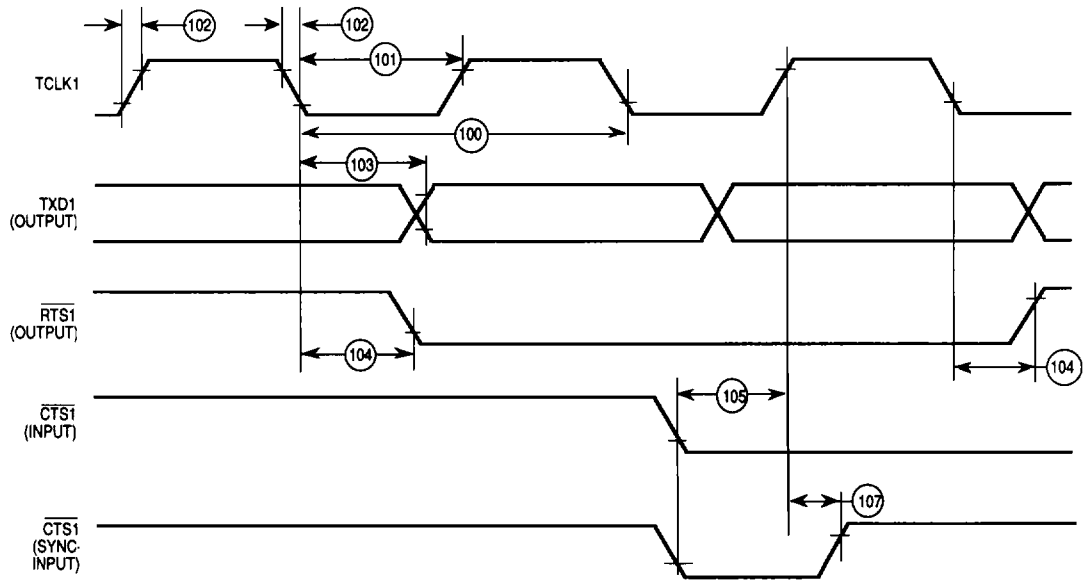


Figure 10-66. SCC NMSI Transmit

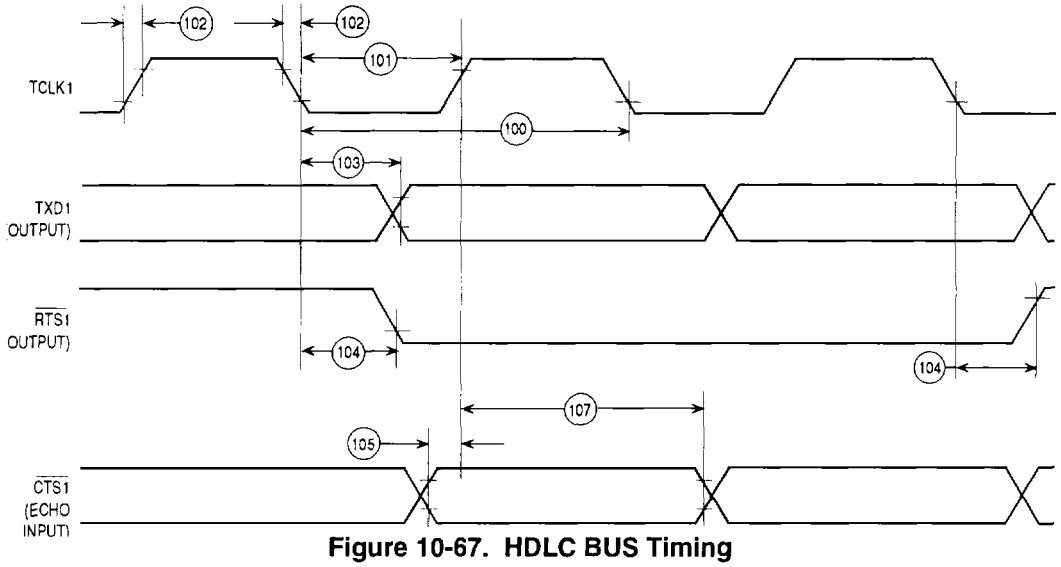


Figure 10-67. HDLC BUS Timing

10.26 ETHERNET ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-68–Figure 10-73)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
120	CLSN Width High	40	—	40	—	ns
121	RCLK1 Rise/Fall Time	—	15	—	15	ns
122	RCLK1 Width Low	CLKO1+ 5ns	—	CLKO1+ 5ns	—	
123[1]	RCLK1 Width high	CLKO1	—	CLKO1	—	
124	RXD1 Setup Time	20	—	20	—	ns
125	RXD1 Hold Time	5	—	5	—	ns
126	RENA Active Delay (from RCLK1 rising edge of the last data bit)	10	—	10	—	ns
127	RENA Width Low	100	—	100	—	ns
128	TCLK1 Rise/Fall Time	—	15	—	15	ns
129	TCLK1 Width Low	CLKO1+ 5ns	—	CLKO1+ 5ns	—	
130[1]	TCLK1 Width high	CLKO1	—	CLKO1	—	
131	TXD1 Active Delay (from TCLK1 rising edge)	10	50	10	50	ns
132	TXD1 Inactive Delay (from TCLK1 rising edge)	10	50	10	50	ns
133	TENA Active Delay (from TCLK1 rising edge)	10	50	10	50	ns
134	TENA Inactive Delay (from TCLK1 rising edge)	10	50	10	50	ns
135	RSTRT Active Delay (from TCLK1 falling edge)	10	50	10	50	ns
136	RSTRT Inactive Delay (from TCLK1 falling edge)	10	50	10	50	ns
137	RRJCT Width Low	1	—	1	—	CLKO1

138[2]	CLKO1 Low to $\overline{SDACK}$ Asserted	—	20	—	20	ns
139[2]	CLKO1 Low to $\overline{SDACK}$ Negated	—	20	—	20	ns

NOTES:
1The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1
2$\overline{SDACK}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

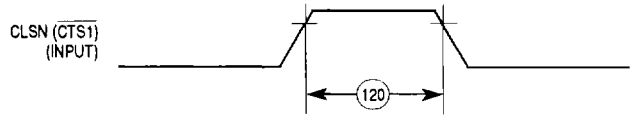


Figure 10-68. Ethernet Collision Timing

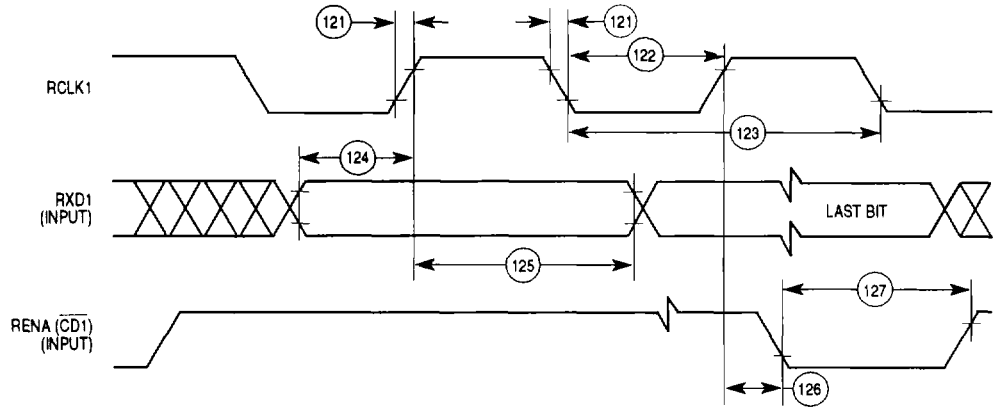
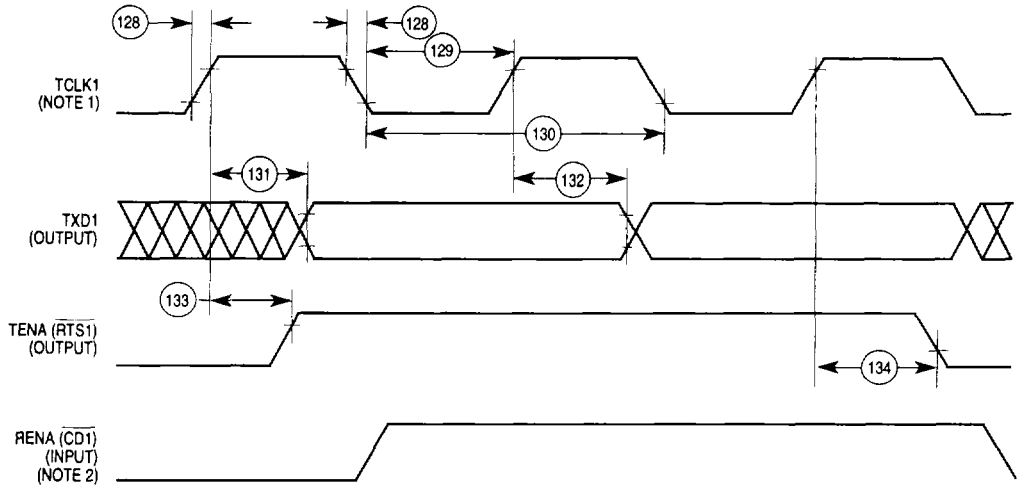


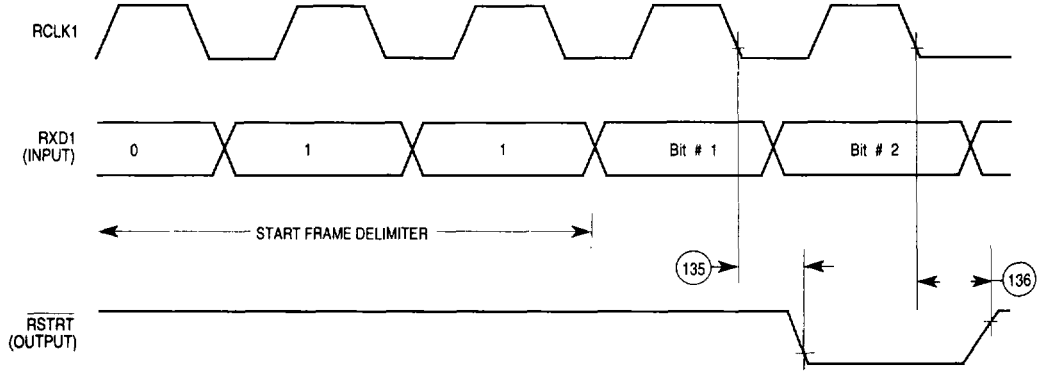
Figure 10-69. Ethernet Receive Timing

10



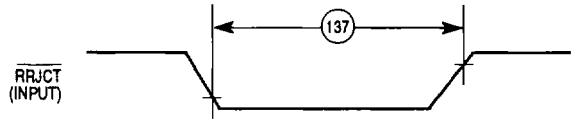
NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transit, then CSL bit is set in the buffer descriptor at the end of frame transmission.

Figure 10-70. Ethernet Transmit Timing



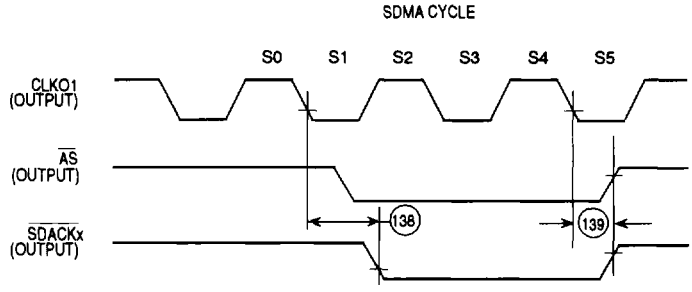
NOTE: Valid for the ethernet protocol only.

Figure 10-71. CAM Interface Receive Start Timing



NOTE: Valid for the ethernet protocol only.

Figure 10-72. CAM Interface Reject Timing



NOTE: SDACKx is asserted when the SDMA writes the received Ethernet frame into memory.

Figure 10-73. SDACK Timing Diagram

10.27 SMC TRANSPARENT MODE ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-74)

10

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
150[1]	SMCLK Clock Period	100	—	100	—	ns
151	SMCLK Width Low	50	—	50	—	ns
151A	SMCLK Width High	50	—	50	—	ns
152	SMCLK Rise/Fall Time	—	15	—	15	ns
153	SMTXD Active Delay (from SMCLK falling edge)	10	50	10	50	ns
154	SMRXD/SYNC1 Setup Time	20	—	20	—	ns
155	SMRXD/SYNC1 Hold Time	5	—	5	—	ns

NOTES:
1.The ratio SyncCLK/SMCLK must be greater or equal to 2/1

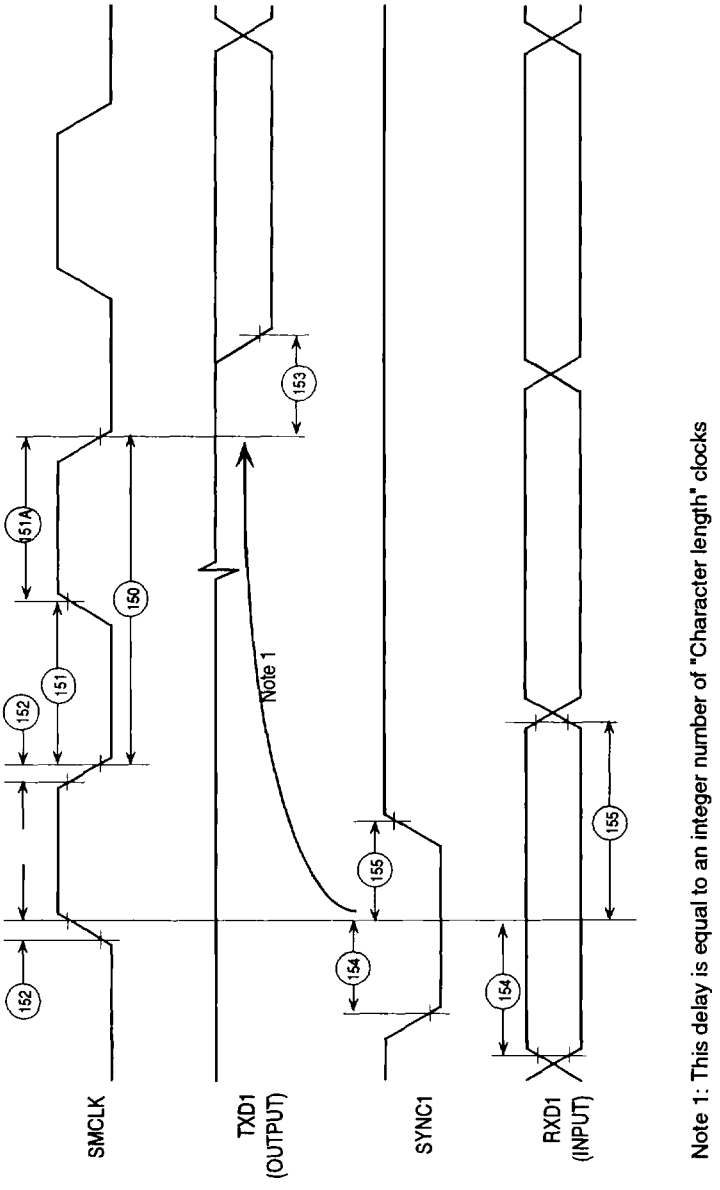


Figure 10-74. SMC Transparent

10.28 SPI MASTER ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-75 and Figure 10-76)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
160	Master Cycle Time	4	1024	4	1024	tcyc
161	Master Clock (SPICLK) High or Low Time	2	512	2	512	tcyc
162	Master Data Setup Time (Inputs)	50	—	50	—	ns
163	Master Data Hold Time (Inputs)	0	—	0	—	ns
164	Master Data Valid (after SPICLK Edge)	—	20	—	20	ns
165	Master Data Hold Time (Outputs)	0	—	0	—	ns
166	Rise Time: Output		15		15	s
167	Fall Time: Output		15		15	ns

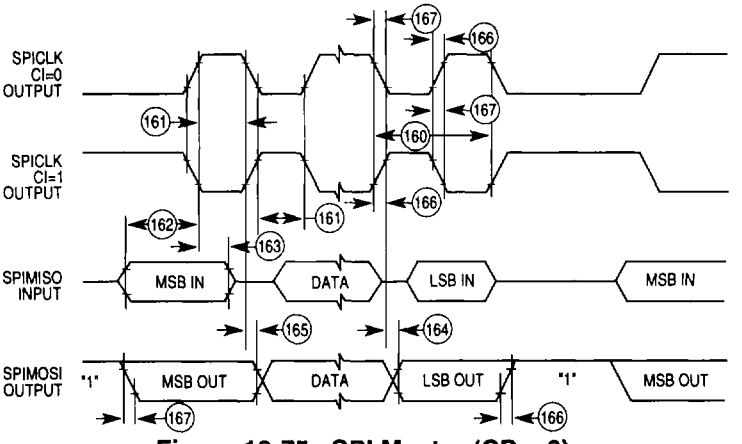


Figure 10-75. SPI Master (CP = 0)

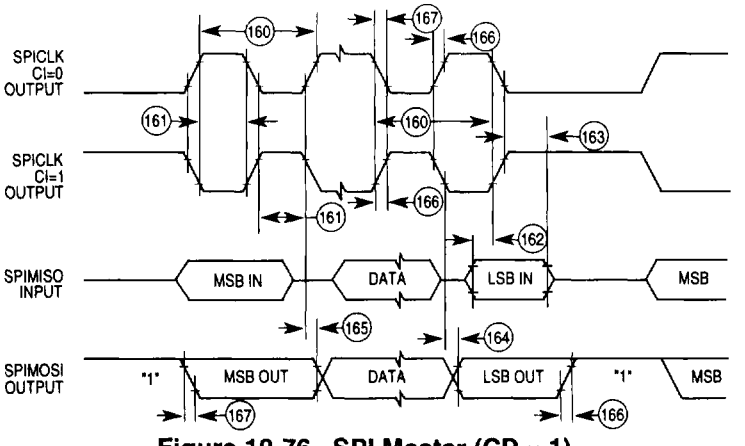


Figure 10-76. SPI Master (CP = 1)

10.29 SPI SLAVE ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-77 and Figure 10-78)

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0 V 33.34 MHz		Unit
		Min	Max	Min	Max	
170	Slave Cycle Time	2	—	2	—	tcyc
171	Slave Enable Lead Time	15		15		ns
172	Slave Enable Lag Time	15		15		ns
173	Slave Clock (SPICLK) High or Low Time	1	—	1	—	tcyc
174	Slave Sequential Transfer Delay (Does Not Require Deselect)	1		1		tcyc
175	Slave Data Setup Time (Inputs)	20	—	20	—	ns
176	Slave Data Hold Time (Inputs)	20	—	20	—	ns
177	Slave Access Time		50		50	ns
178	Slave SPIMISO Disable Time		50		50	ns
179	Slave Data Valid (after SPICLK Edge)	—	50	—	50	ns
180	Slave Data Hold Time (Outputs)	0	—	0	—	ns
181	Rise Time: Input		15		15	ns
182	Fall Time: Input		15		15	ns

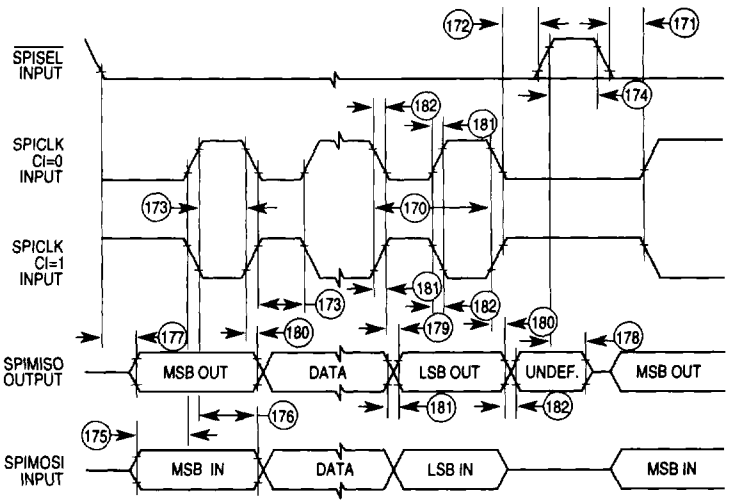


Figure 10-77. SPI Slave (CP = 0)

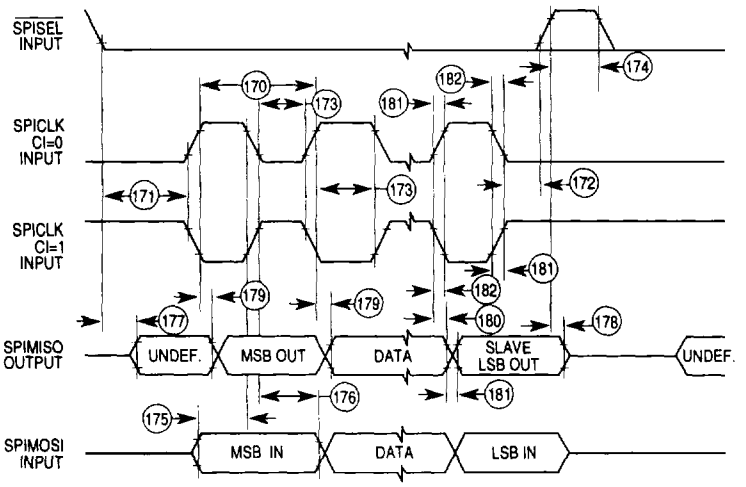


Figure 10-78. SPI Slave (CP = 1)

10.30 JTAG ELECTRICAL SPECIFICATIONS

(The electrical specifications in this document are preliminary. See Figure 10-79–Figure 10-82)

Num.	Characteristic	3.3 V or 5.0 V		5.0 V		Unit
		25.0 MHz		33.3MHz		
		Min	Max	Min	Max	
	TCK Frequency of Operation	0	25	0	25	MHz
1	TCK Cycle Time in Crystal Mode	40	—	40	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	18	—	18	—	ns
3	TCK Rise and Fall Times	0	3	0	3	ns
6	Boundary Scan Input Data Setup Time	10	—	10	—	ns
7	Boundary Scan Input Data Hold Time	18	—	18	—	ns
8	TCK Low to Output Data Valid	0	30	0	30	ns
9	TCK Low to Output High Impedance	0	40	0	40	ns
10	TMS, TDI Data Setup Time	10	—	10	—	ns
11	TMS, TDI Data Hold Time	10	—	10	—	ns
12	TCK Low to TDO Data Valid	0	20	0	20	ns
13	TCK Low to TDO High Impedance	0	20	0	20	ns
14	$\overline{TRST}$ Assert Time	100	—	100	—	ns
15	$\overline{TRST}$ Setup Time to TCK Low	40	—	40	—	ns

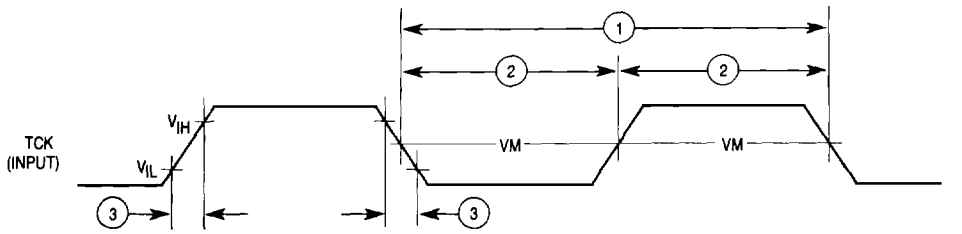


Figure 10-79. Test Clock Input Timing Diagram

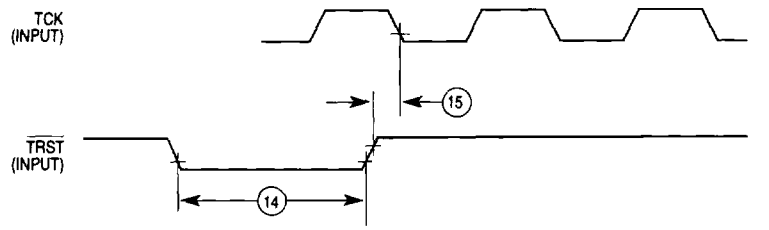


Figure 10-80. $\overline{TRST}$ Timing Diagram

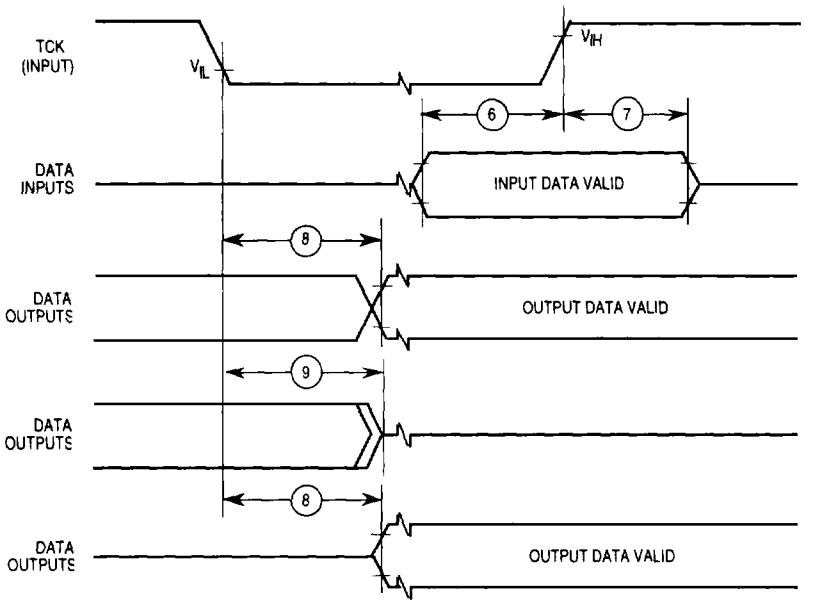


Figure 10-81. Boundary Scan (JTAG) Timing Diagram

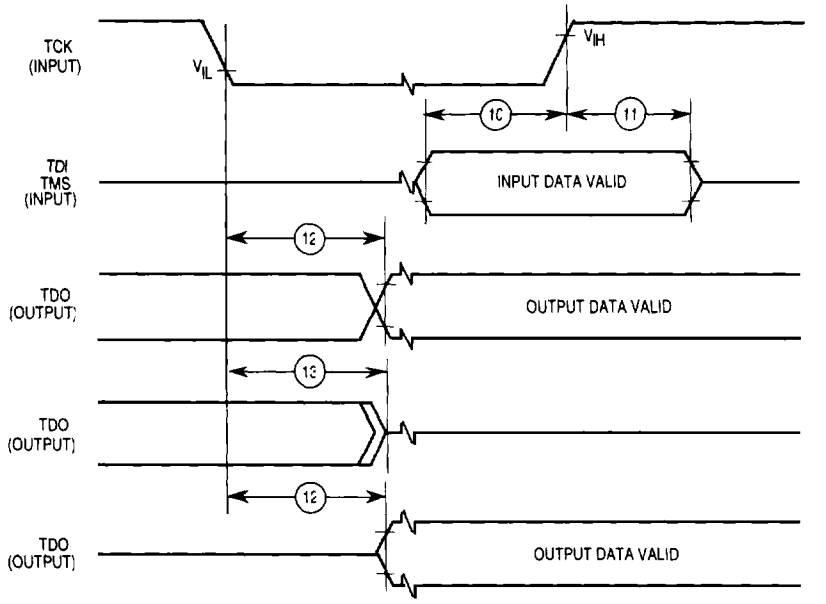


Figure 10-82. Test Access Port Timing Diagram