LMC567 Low Power Tone Decoder

Check for Samples: LMC567

FEATURES

- **Functionally Similar to LM567**
- **2V to 9V Supply Voltage Range**
- **Low Supply Current Drain**
- **No Increase in Current with Output Activated**
- **Operates to 500 kHz Input Frequency**
- **High Oscillator Stability**
- **Ground-referenced Input**
- **Hysteresis Added to Amplitude Comparator**
- **Out-of-band Signals and Noise Rejected**
- **20 mA Output Current Capability**

DESCRIPTION

The LMC567 is a low power general purpose LMCMOS tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Block Diagram

(with External Components)
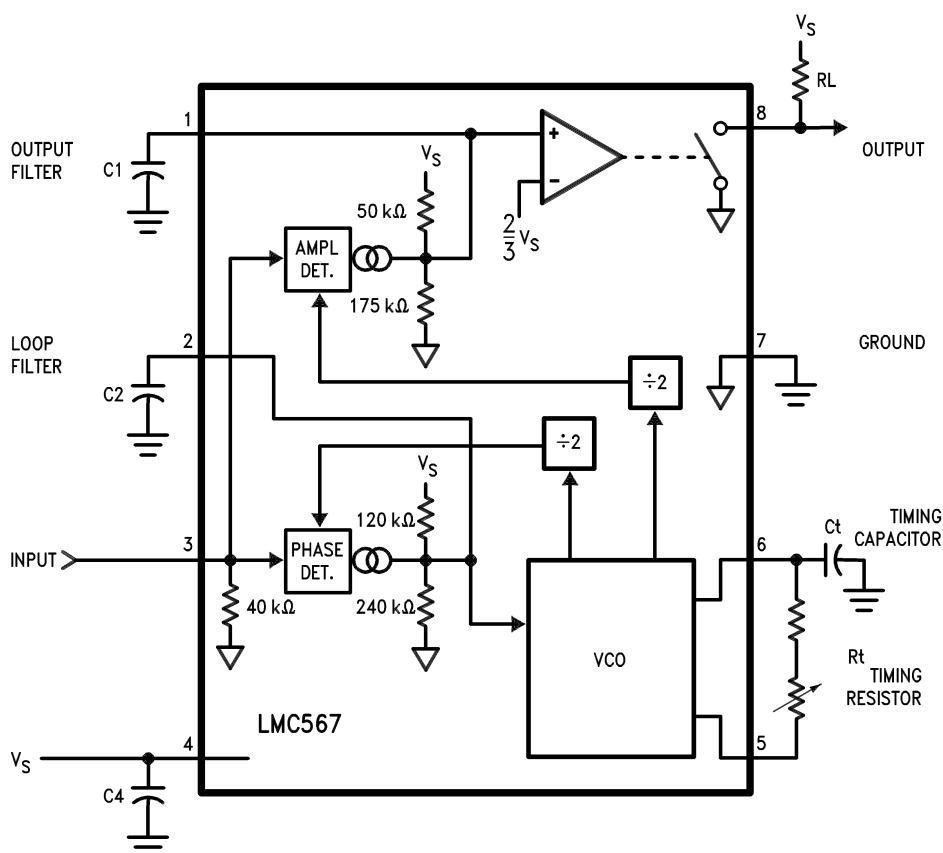
Figure 1. See Package Number D0008A or P0008E

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

LMC567

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

	MIN	MAX	UNIT
Input Voltage, Pin 3	2		V_{p-p}
Supply Voltage, Pin 4		10	
Output Voltage, Pin 8		13	V
Voltage at All Other Pins, Vs to Gnd			
Output Current, Pin 8		30	mA
Package Dissipation		500	mW
Operating Temperature Range (T_A)	−25	125	
Storage Temperature Range	−55	150	°C
Soldering Information[(3)] **PDIP Package**			
Soldering (10 sec.)		260	°C
SOIC Package			
Vapor Phase (60 sec.)		215	
Infrared (15 sec.)		220	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) See http://www.ti.com for other methods of soldering surface mount devices.

ELECTRICAL CHARACTERISTICS

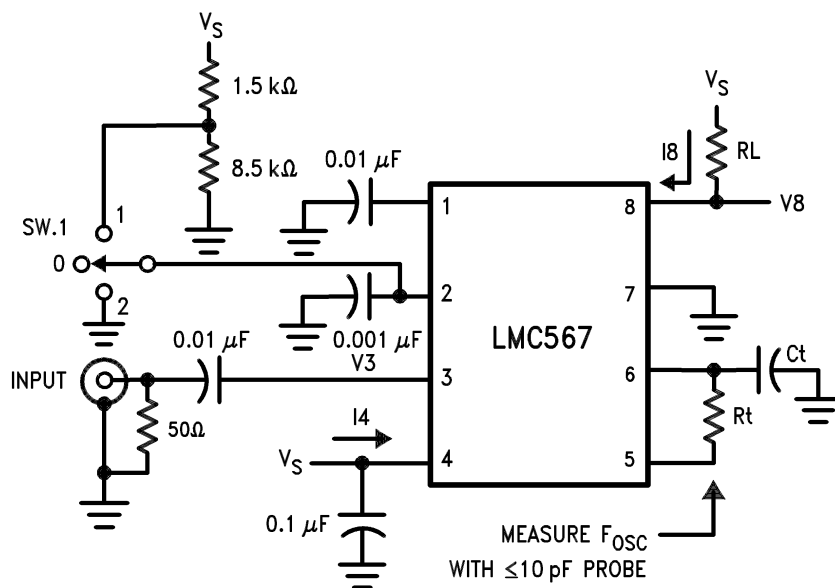Test Circuit, T_A = 25°C, V_s = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_s = 2V		0.3		mAdc
			V_s = 5V		0.5	0.8	
			V_s = 9V		0.8	1.3	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency, $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_s = 2V		98		kHz
			V_s = 5V	92	103	113	
			V_s = 9V		105		
Δf_0	Center Frequency Shift with Supply	$$\frac{f_0|_{9V} - f_0|_{2V}}{7\,f_0|_{5V}} \times 100$$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level Until Pin 8 Goes Low.	V_s = 2V	11	20	27	mVrms
			V_s = 5V	17	30	45	
			V_s = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High.			1.5		mVrms
V8	Output "Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		

Product Folder Links: LMC567

ELECTRICAL CHARACTERISTICS (continued)

Test Circuit, T_A = 25°C, V_s = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; $$L.D.B.W. = \frac{F_{osc}|P2 - F_{osc}|P1}{F_{osc}|P0} \times 100$$	V_s = 2V	7	11	15	%
			V_s = 5V	11	14	17	
			V_s = 9V		15		
ΔBW	Bandwidth Skew	$$Skew = \left(\frac{F_{osc}|P2 - F_{osc}|P1}{2\,F_{osc}|P0} - 1\right) \times 100$$			0	±1.0	%
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz
V_{in}	Input Threshold at f_{max}	Set Input Frequency Equal to f_{max} measured Above, Increase Input Level Until Pin 8 goes Low.			35		mVrms

Test Circuit

RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current
vs.
Operating Frequency**

Figure 2.

**Bandwidth
vs.
Input Signal Level**

Figure 3.

**Largest Detection
Bandwidth
vs.
Temp.**

Figure 4.

**Bandwidth as
a Function of C2**

Figure 5.

**Frequency Drift
with Temperature**

Figure 6.

**Frequency Drift
with Temperature**
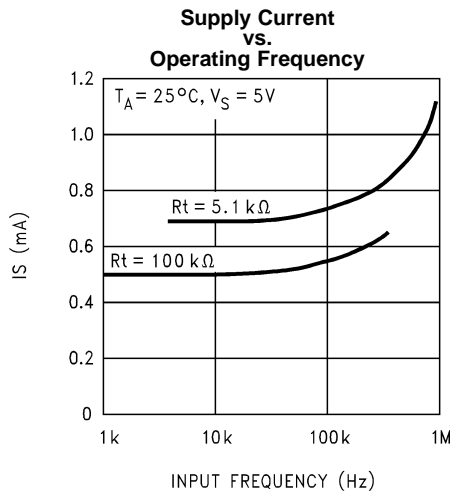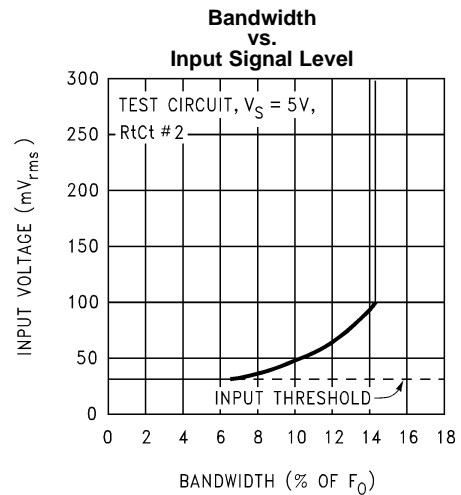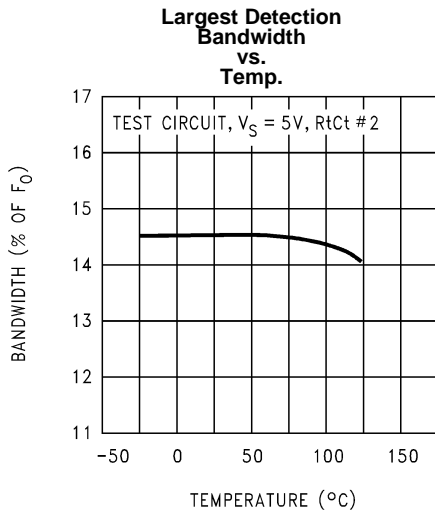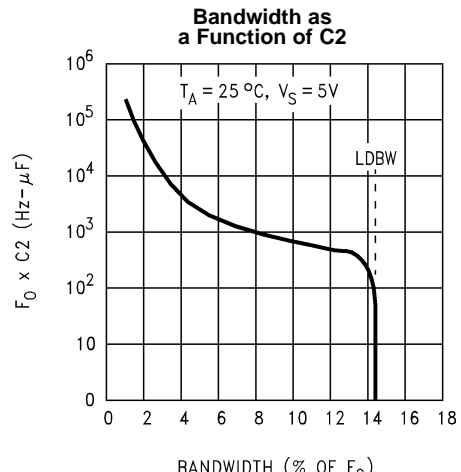
Figure 7.
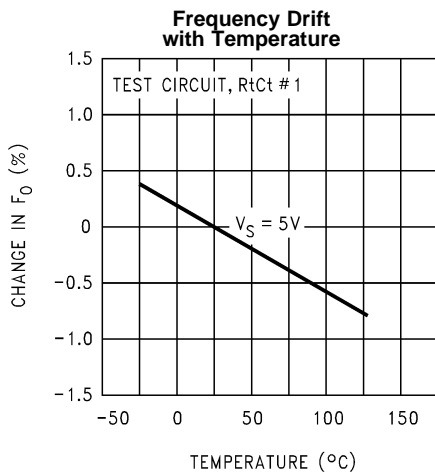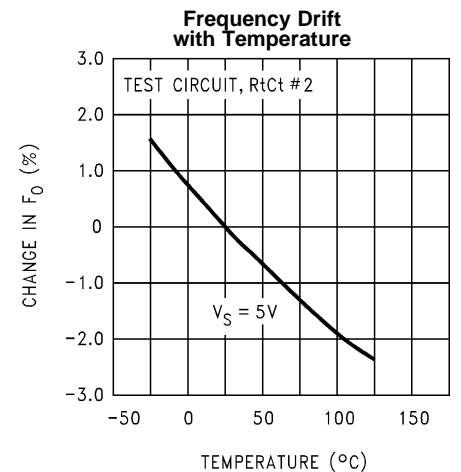
Product Folder Links: *LMC567*

APPLICATION INFORMATION

(refer to Block Diagram)

GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{OSC} \cong \frac{1}{1.4\ R_tC_t}\ Hz \tag{1}$$

Since this will cause an input tone of half F_{osc} to be decoded,

$$F_{INPUT} \cong \frac{1}{2.8\ R_tC_t}\ Hz \tag{2}$$

This equation is accurate at low frequencies; however, above 50 kHz (F_{osc} = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to V_s every half cycle to charge Ct:

I_s due to Rt = $V_s/(4R_t)$ (3)

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_s. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 V_s the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 V_s. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the "sat" voltage for a given output current will increase at lower supplies.

Product Folder Links: *LMC567*

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC567CM	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 100	LMC 567CM	Samples
LMC567CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 100	LMC 567CM	Samples
LMC567CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 100	LMC 567CM	Samples
LMC567CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-25 to 100	LMC 567CN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC567CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC567CMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92)
MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001 variation BA.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE
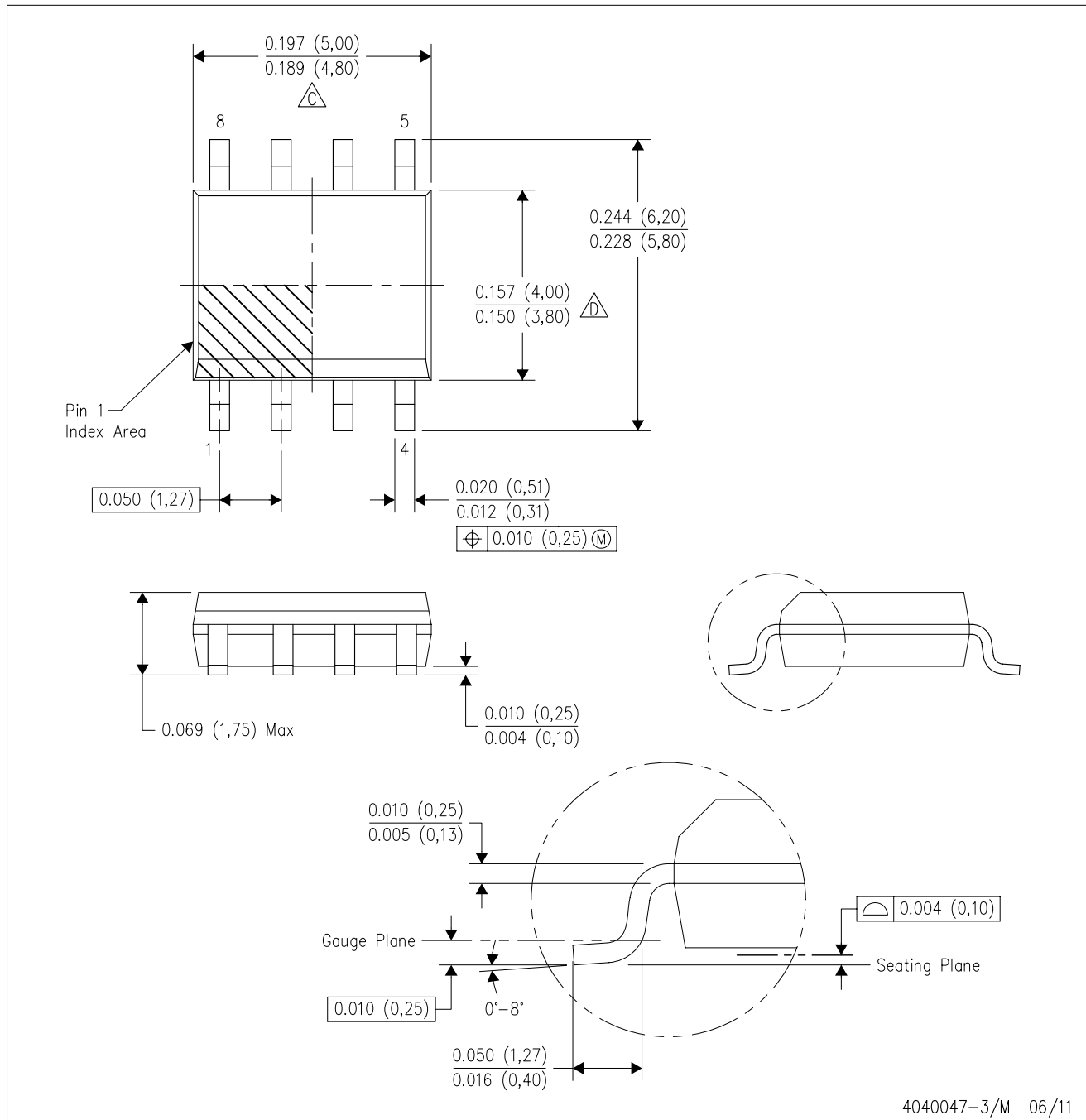
0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   △D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
      △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
      △D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		