



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-243AA*	TO-39	TO-92
-40V	25 Ω	-0.25A	—	VP1304N2	VP1304N3
-60V	25 Ω	-0.25A	—	VP1306N2	VP1306N3
-100V	25 Ω	-0.25A	VP1310N8	VP1310N2	VP1310N3

*Same as SOT-89. For carrier tape reels specify P023 for 1,000 units or P024 for 2,000 units.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

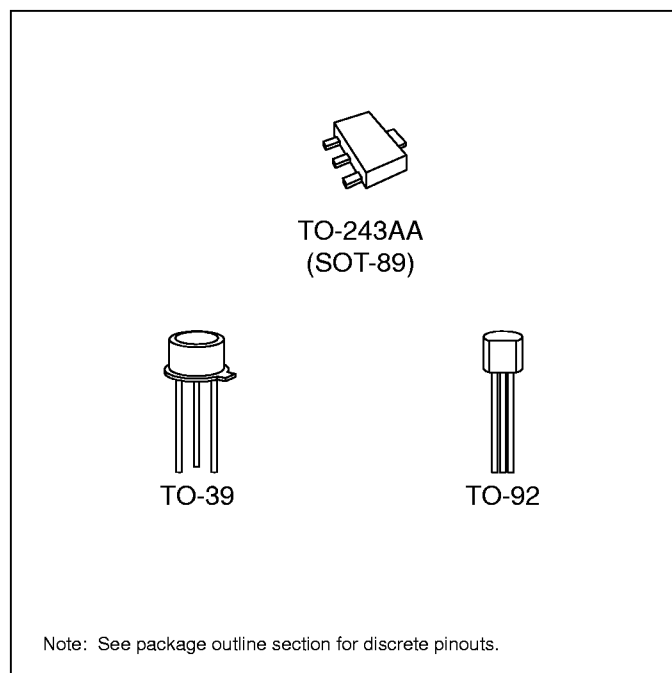
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{ja} $^\circ\text{C/W}$	θ_{jc} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
SOT-89	-0.20A	-0.70A	1.6W†	78	15	-0.20A	-0.70A
TO-39	-0.25A	-0.80A	3.0W	125	41	-0.25A	-0.80A
TO-92	-0.15A	-0.65A	1.0W	170	125	-0.15A	-0.65A

* I_D (continuous) is limited by max rated T_J , $T_A = 25^\circ\text{C}$

† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

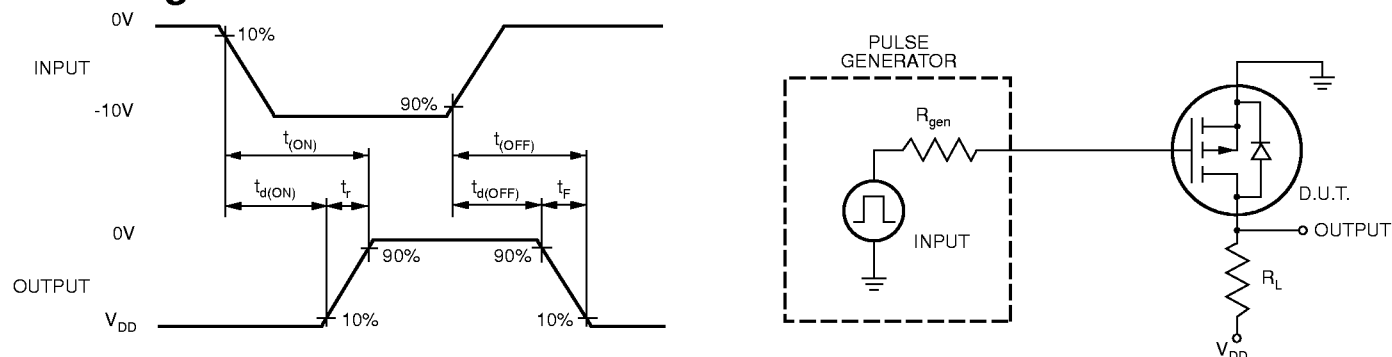
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1310	-100		V	$I_D = -1\text{mA}$, $V_{GS} = 0\text{V}$
		VP1306	-60			
		VP1304	-40			
$V_{GS(th)}$	Gate Threshold Voltage	-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.2	-3.85	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}$, $I_D = -1\text{mA}$
I_{GSS}	Gate Body Leakage		-0.1	-100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	$V_{GS} = 0\text{V}$, $V_{DS} = \text{Max Rating}$
				-500		$V_{GS} = 0\text{V}$, $V_{DS} = 0.8 \text{ Max Rating}$, $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.08	-0.23		A	$V_{GS} = -5\text{V}$, $V_{DS} = -25\text{V}$
		-0.25	-0.7			$V_{GS} = -10\text{V}$, $V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		32	40	Ω	$V_{GS} = -5\text{V}$, $I_D = -50\text{mA}$
			19	25		$V_{GS} = -10\text{V}$, $I_D = -250\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.8	1.1	%/ $^\circ\text{C}$	$I_D = -250\text{mA}$, $V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance	75	120		mS	$V_{DS} = -25\text{V}$, $I_D = -200\text{mA}$
C_{ISS}	Input Capacitance		20	35	pF	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		12	15		
C_{RSS}	Reverse Transfer Capacitance		3	5		
$t_{d(ON)}$	Turn-ON Delay Time		3	5	ns	$V_{DD} = -25\text{V}$ $I_D = -250\text{mA}$ $R_{GEN} = 25\Omega$
t_r	Rise Time		3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time		3	5		
t_f	Fall Time		3	8		
V_{SD}	Diode Forward Voltage Drop		-1.2	-1.7	V	$I_{SD} = -0.25\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time		350		ns	$I_{SD} = -0.25\text{A}$, $V_{GS} = 0\text{V}$

Notes:

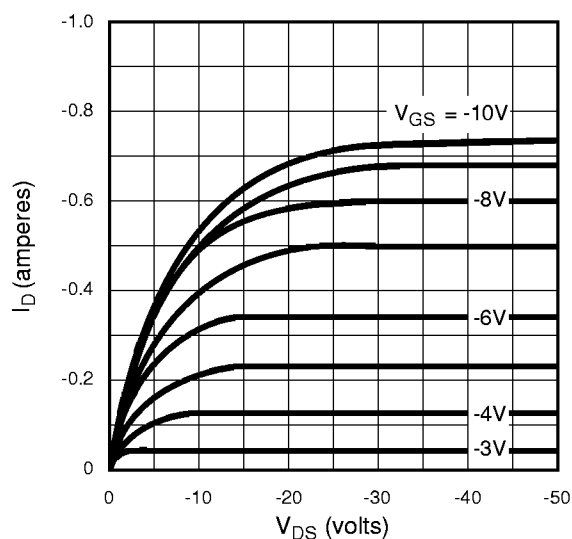
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

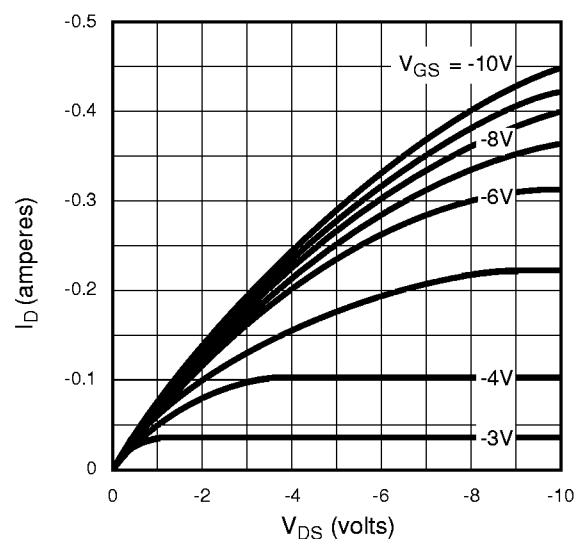


Typical Performance Curves

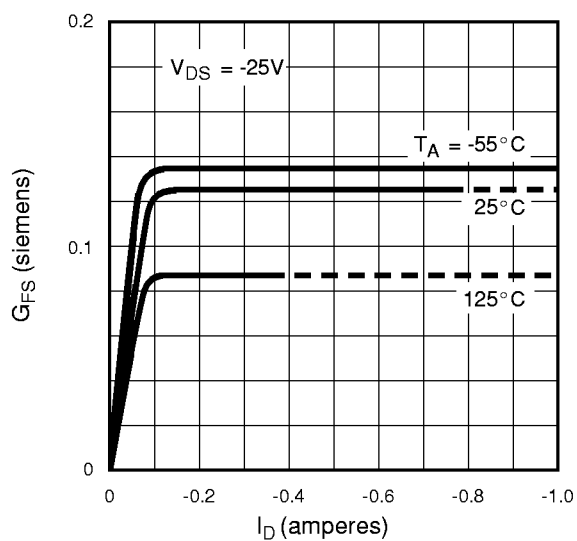
Output Characteristics



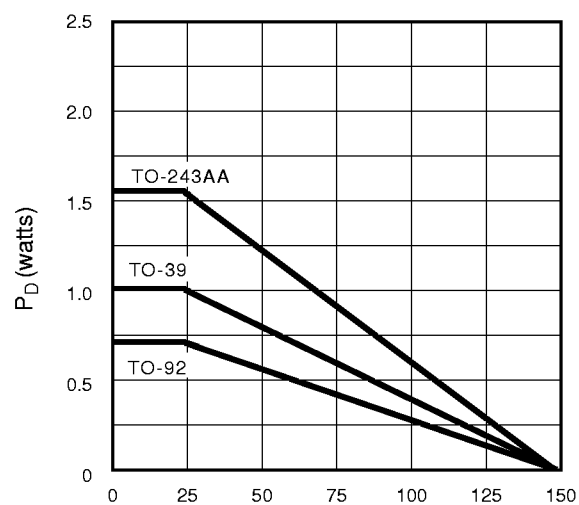
Saturation Characteristics



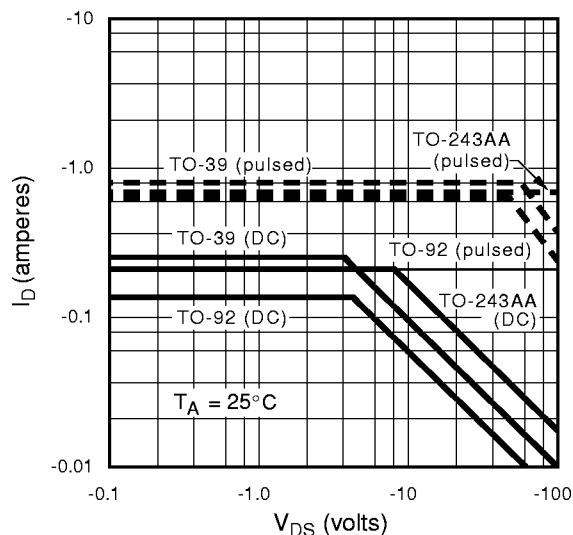
Transconductance vs. Drain Current



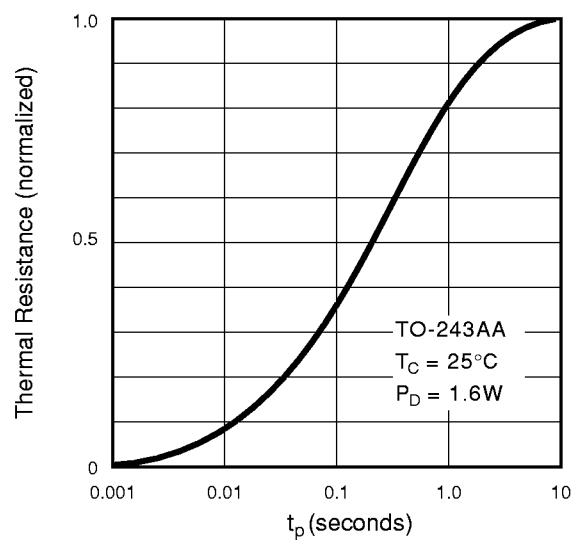
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

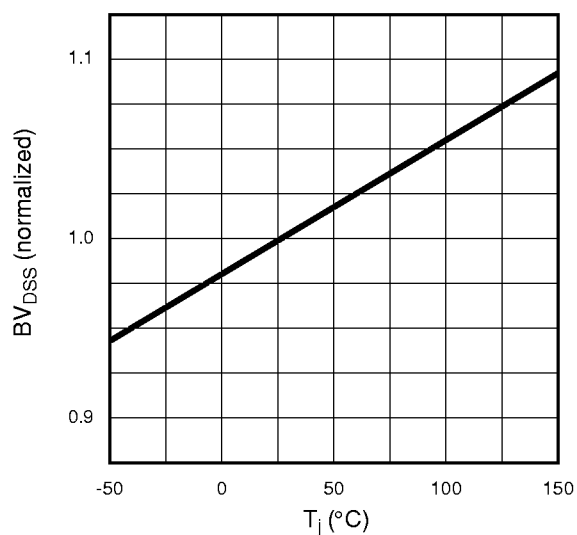


Thermal Response Characteristics

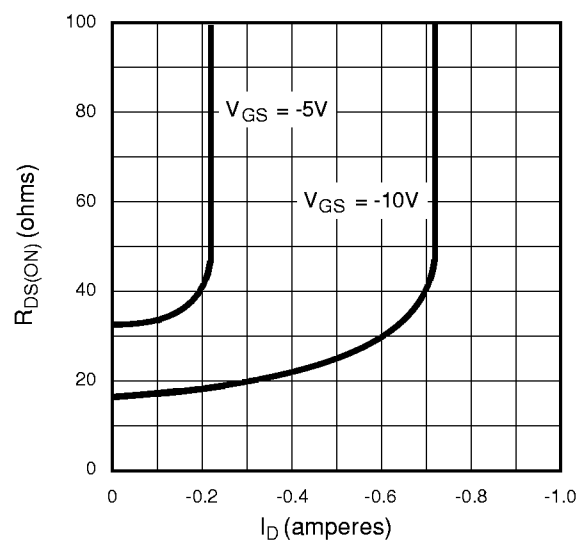


Typical Performance Curves

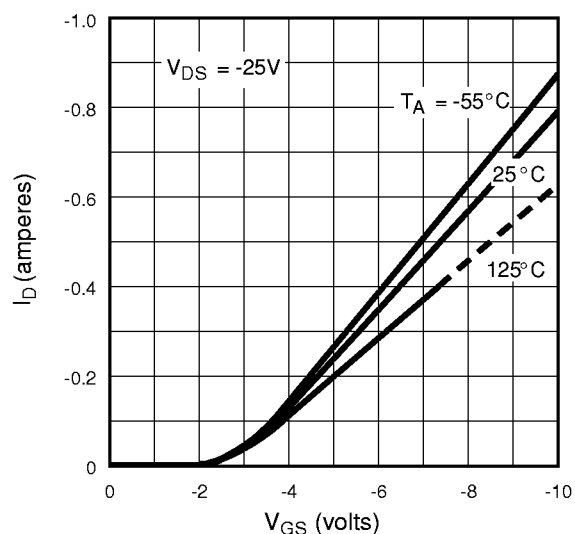
BV_{DSS} Variation with Temperature



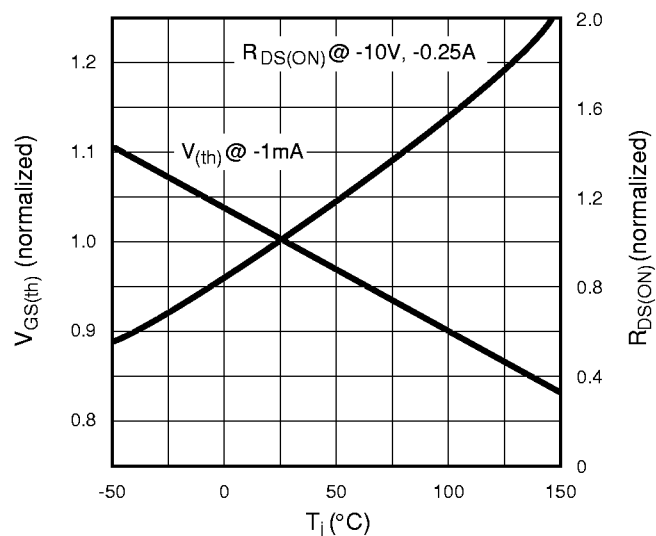
On-Resistance vs. Drain Current



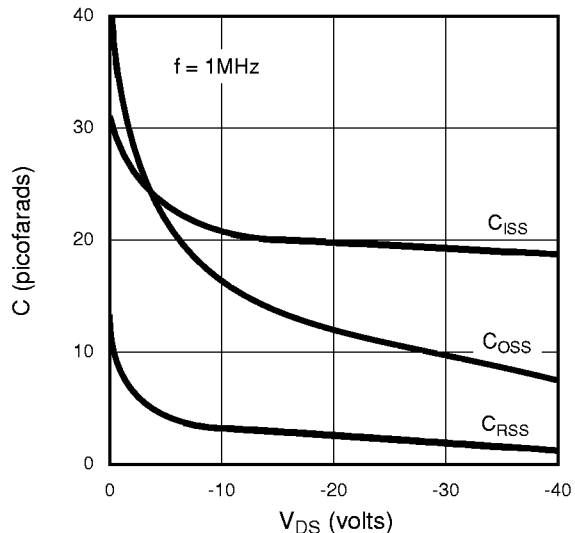
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

