XC3000
Logic Cell™ Array Family

Product Specification

FEATURES

- High Performance—50, 70 and 100 MHz Toggle Rates
- Second Generation User-Programmable Gate Array
  - I/O functions
  - Digital logic functions
  - Interconnections
- Flexible array architecture
  - Compatible arrays, 2000 to 9000 gate logic complexity
  - Extensive register and I/O capabilities
  - High fan-out signal distribution
  - Internal three-state bus capabilities
  - TTL or CMOS input thresholds
  - On-chip oscillator amplifier
- Standard product availability
  - Low power, CMOS, static memory technology
  - Performance equivalent to TTL SSI/MSI
  - 100% factory pre-tested
  - Selectable configuration modes
- Complete XACT™ development system
  - Schematic Capture
  - Automatic Place/Route
  - Logic and Timing Simulation
  - Design Editor
  - Library and User Macros
  - Timing Calculator
  - XACTOR In-Circuit Verifier
  - Standard PROM File Interface

DESCRIPTION

The CMOS XC3000 Logic Cell™ Array (LCA) family provides a group of high-performance, high-density, digital, integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks, a core array of Logic Blocks and resources for interconnection. The general structure of a Logic Cell Array is shown in Figure 1 on the next page. The XACT development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimizaton, and to compile the data pattern which represents the configuration program.

The Logic Cell Array's user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. Xilinx's companion XC1736 Serial Configuration PROM provides a very simple serial configuration program storage in a one-time-programmable eight-pin DIP.

Basic Array	Logic Capacity (usable gates)	Configurable Logic Blocks	User I/Os	Program Data (bits)
XC3020	2000	64	64	14779
XC3030	3000	100	80	22176
XC3042	4200	144	96	30784
XC3064	6400	224	120	46064
XC3090	9000	320	144	64160

The XC3000 Logic Cell Arrays are an enhanced family of Programmable Gate Arrays, which provide a variety of logic capacities, package styles, temperature ranges and speed grades.

ARCHITECTURE

The perimeter of configurable I/O Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The blocks' logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass tran-

sistors. These functions of the Logic Cell Array are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the Logic Cell Array at power-up and may be reloaded on command. The Logic Cell Array includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The XACT development system generates the configuration program bit-stream used to configure the Logic Cell Array. The memory loading process is independent of the user logic functions.

CONFIGURATION MEMORY

The static memory cell used for the configuration memory in the Logic Cell Array has been designed specifically for high reliability and noise immunity. Integrity of the LCA configuration memory based on this design is assured even under adverse conditions. Compared with other programming alternatives, static memory provides the best combination of high density, high performance, high reliability and comprehensive testability. As shown in Figure 2, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation the cell provides continuous control and the pass transistor is "off" and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and re-written.

The memory cell outputs Q and $\overline{Q}$ use full Ground and Vcc levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the

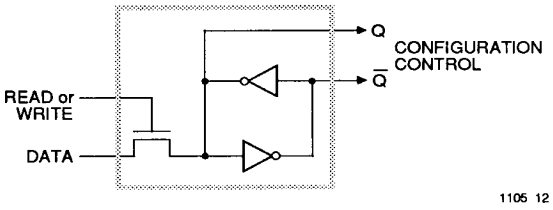

Figure 2. A static configuration memory cell is loaded with one bit of configuration program and controls one program selection in the Logic Cell Array.

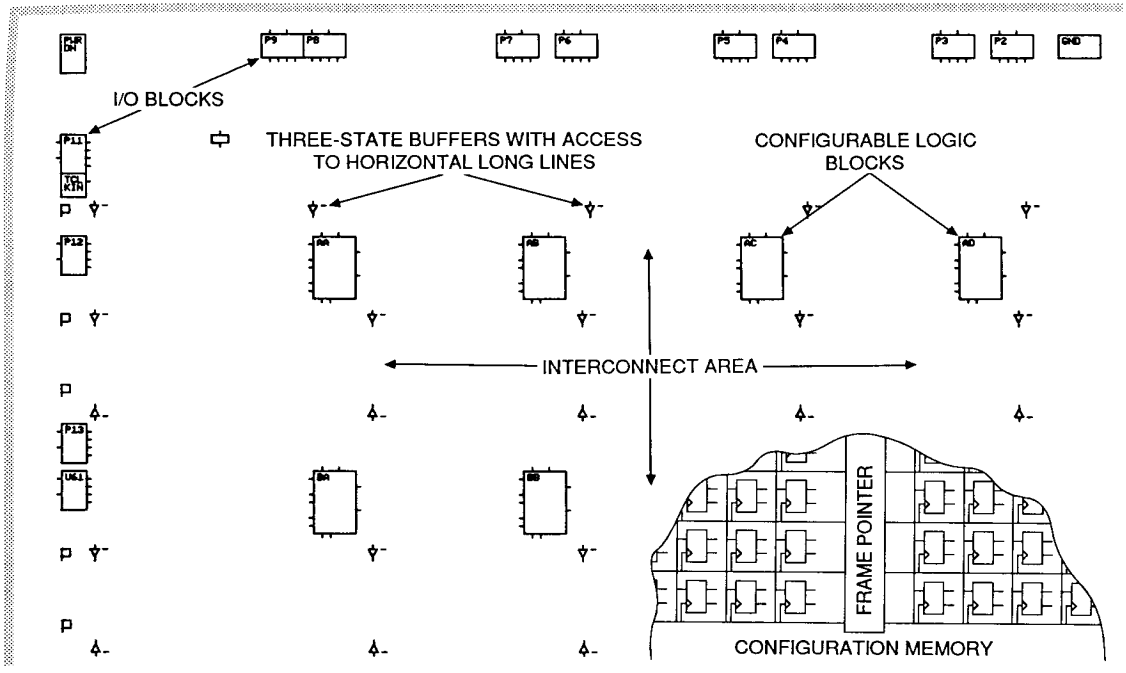

Figure 1. The structure of the Logic Cell Array consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

cell. Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. In reliability testing no soft errors have been observed, even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte wide data. The internal configuration logic utilizes framing information, embedded in the program data by the XACT development system, to direct memory cell loading. The serial data framing and length count preamble provide programming compatibility for mixes of various Xilinx programmable gate arrays in a synchronous, serial, daisy-chain fashion.

I/O BLOCK

Each user-configurable I/O Block (IOB), shown in Figure 3, provides an interface between the external package pin of the device and the internal user logic. Each I/O Block includes both registered and direct input paths. Each IOB provides a programmable three-state output buffer which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electro-static protection, and circuits to inhibit latch-up produced by input currents.

The input buffer portion of each I/O Block provides thresh-

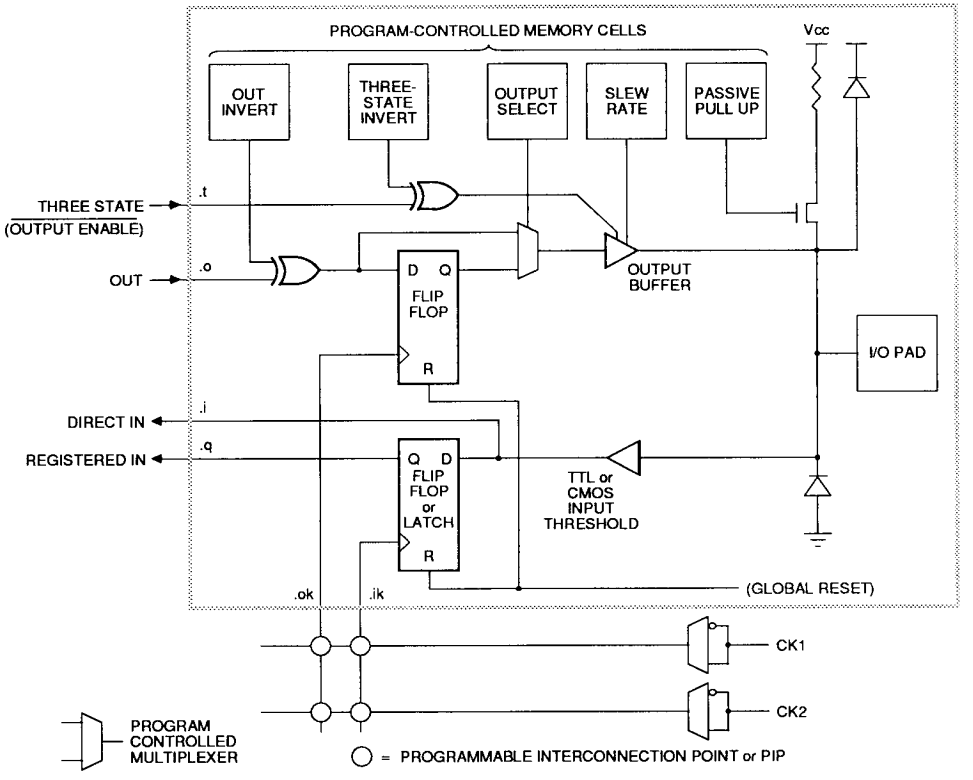

Figure 3. The Input/Output Block includes input and output storage elements and I/O options selected by configuration memory cells.
A choice of two clocks is available on each die edge.
The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa.
Passive Pull-up can only be enabled on inputs, not on outputs.
All user inputs are programmed for TTL or CMOS thresholds.

old detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the I/O Blocks can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element which may be configured as a positive edge-triggered "D" flip-flop or a low level-transparent latch. The sense of the clock can be inverted (negative edge/high transparent) as long as all IOBs on the same clock net use the same clock sense. Clock/load signals (I/O Block pins *.ik* and *.ok*) can be selected from either of two die edge metal lines. I/O storage elements are reset during configuration or by the active low chip $\overline{\text{RESET}}$ input. Both direct input [from I/O Block pin *.i*] and registered input [from I/O Block pin *.q*] signals are available for interconnect.

For reliable operation inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user I/O Block includes a programmable high impedance pull-up resistor which may be selected by the program to provide a constant HIGH for otherwise undriven package pins. Although the Logic Cell Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the I/O Block and logic block flip-flops are about 3 nanoseconds. This short delay provides good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition which can result from assertion of the clock during data transitions. Because of the short loop delay characteristic in the Logic Cell Array, the I/O Block flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the I/O Block, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the I/O Blocks provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving I/O Block pin .o becomes the registered or direct data source for the output buffer. The three-state control signal [I/O Block pin *.t*] can control output activity. An open-drain type output may be obtained by using the same signal for driving the output and three-state signal nets so that the buffer output is enabled only for a LOW.

Configuration program bits for each I/O Block control features such as optional output register, logical signal inversion, and three-state and slew rate control of the output.

The program-controlled memory cells of Figure 3 control the following options:

- Logical **inversion of the output** is controlled by one configuration program bit per I/O Block.

- Logical **three-state control** of each I/O Block output buffer is determined by the states of configuration program bits which turn the buffer on, or off, or select the output buffer three-state control interconnection [I/O Block pin *.t*]. When this I/O Block output control signal is HIGH, a logic "1", the buffer is **disabled** and the package pin is high impedance. When this I/O block output control signal is LOW, a logic "0", the buffer is **enabled** and the package pin is active. Inversion of the buffer three-state control logic sense (output enable) is controlled by an additional configuration program bit.

- **Direct or registered output** is selectable for each I/O block. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied [I/O Block pin *.ok*] by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.

- **Increased output transition speed** can be selected to improve critical timing. Slower transitions reduce capacitive load peak currents of non-critical outputs and minimize system noise.

- A high impedance **pull-up resistor** may be used to prevent unused inputs from floating.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit

- Outputs
  - Direct/registered
  - Inverted/not
  - Three-state/on/off
  - Full speed/slew limited
  - Three-state/output enable (inverse)

CONFIGURABLE LOGIC BLOCK

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of I/O Blocks. The XC3020 has 64 such blocks arranged in 8 rows and 8 columns. The XACT development system is used to compile the configuration data which are to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of configurable logic blocks and their interconnecting networks may be done by automatic translation from a schematic capture logic diagram or optionally by installing library or user macros.

Each configurable logic block has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 4. There are: five logic inputs [*.a, .b, .c, .d* and *.e*]; a common clock input [*.k*]; an asynchronous direct reset input [*.rd*]; and an enable clock [*.ec*]. All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs [*.x* and *.y*] which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, data-in [*.di*]. Both flip-flops in each CLB share the asynchronous reset [*.rd*] which, when enabled and HIGH, is dominant over clocked inputs. All flip-flops are

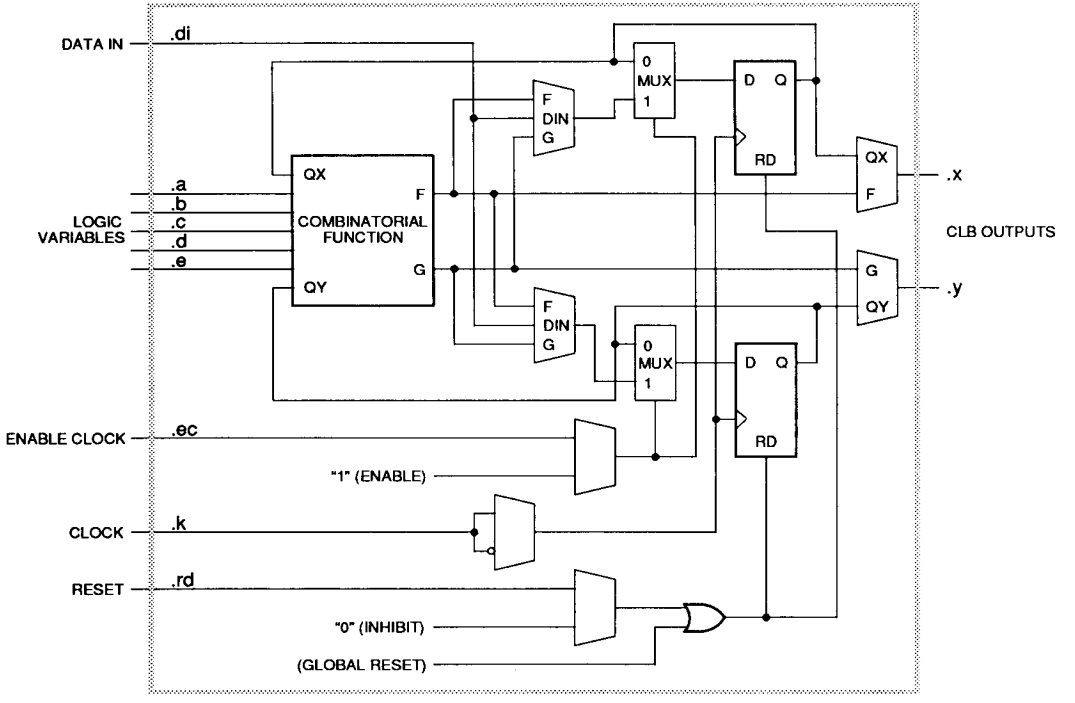

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Figure 4. Each Configurable Logic Block includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function.

It has: five logic variable inputs .a, .b, .c, .d and .e.
a direct data in .di
an enable clock .ec
a clock (invertible) .k
an asynchronous reset .rd
two outputs .x and .y

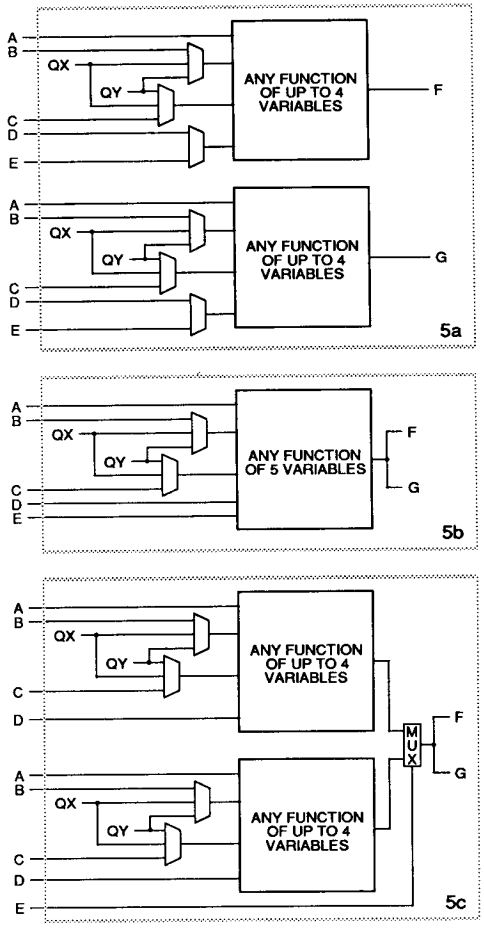

Figure 5

5a. Combinatorial Logic Option 1 generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of of B, C, Qx and Qy. The fourth variable can be any choice of D or E.

5b. Combinatorial Logic Option 2 generates any function of five variables: A, D, E and and two choices out of B, C, Qx, Qy.

5c. Combinatorial Logic Option 3 allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, Qx and Qy for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

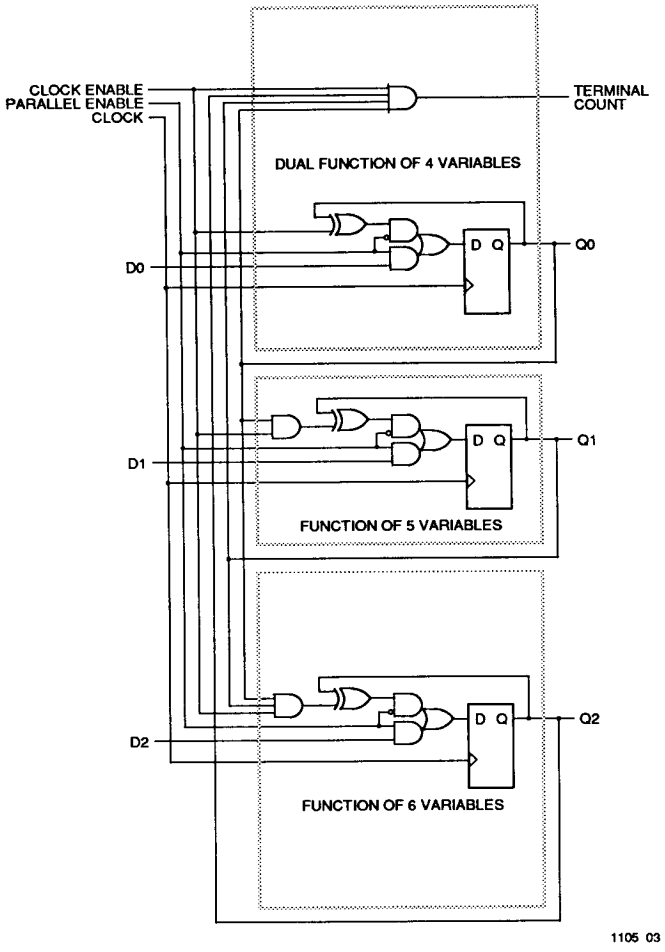

Figure 6. The C8BCP macro (modulo 8 binary counter with parallel enable and clock enable) uses one combinatorial logic block of each option.

reset by the active low chip input, $\overline{\text{RESET}}$, or during the configuration process. The flip-flops share the enable clock [*.ec*] which, when LOW, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input [*.k*], as well as its active sense within each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinatorial logic portion of the logic block uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 5a, or a single function of five variables as shown in Figure 5b, or some functions of seven variables as shown in Figure 5c. Figure 6 shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable [*.e*] to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the logic blocks and I/O Blocks.

PROGRAMMABLE INTERCONNECT

Programmable Interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logical networks. Interconnections between blocks are composed from a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 7 is an example of a routed net. The XACT development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the logic or I/O Blocks are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. ***As the switch connections to block inputs are unidirectional (as are block outputs) they are usable only for block input connection and not routing.*** Figure 8 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines (multiplexed busses and wide AND gates)

General Purpose Interconnect

General purpose interconnect, as shown in Figure 9, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and I/O Blocks. Each segment is the "height" or "width" of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by using "Editnet" to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 10 and may be highlighted by the use of the show matrix command in XACT.

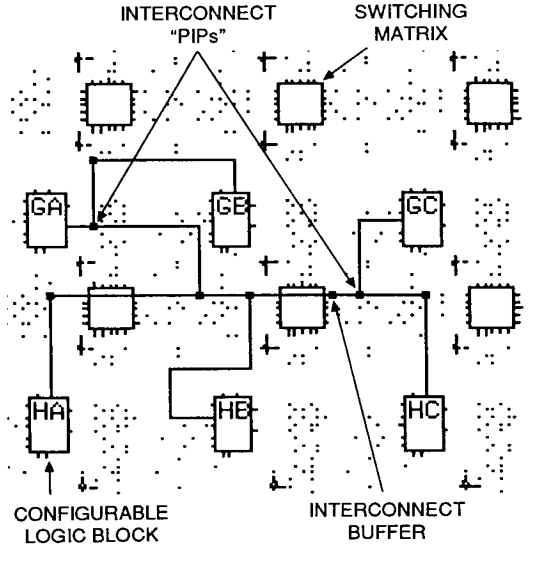

Figure 7. An XACT view of routing resources used to form a typical interconnection network from CLB GA.

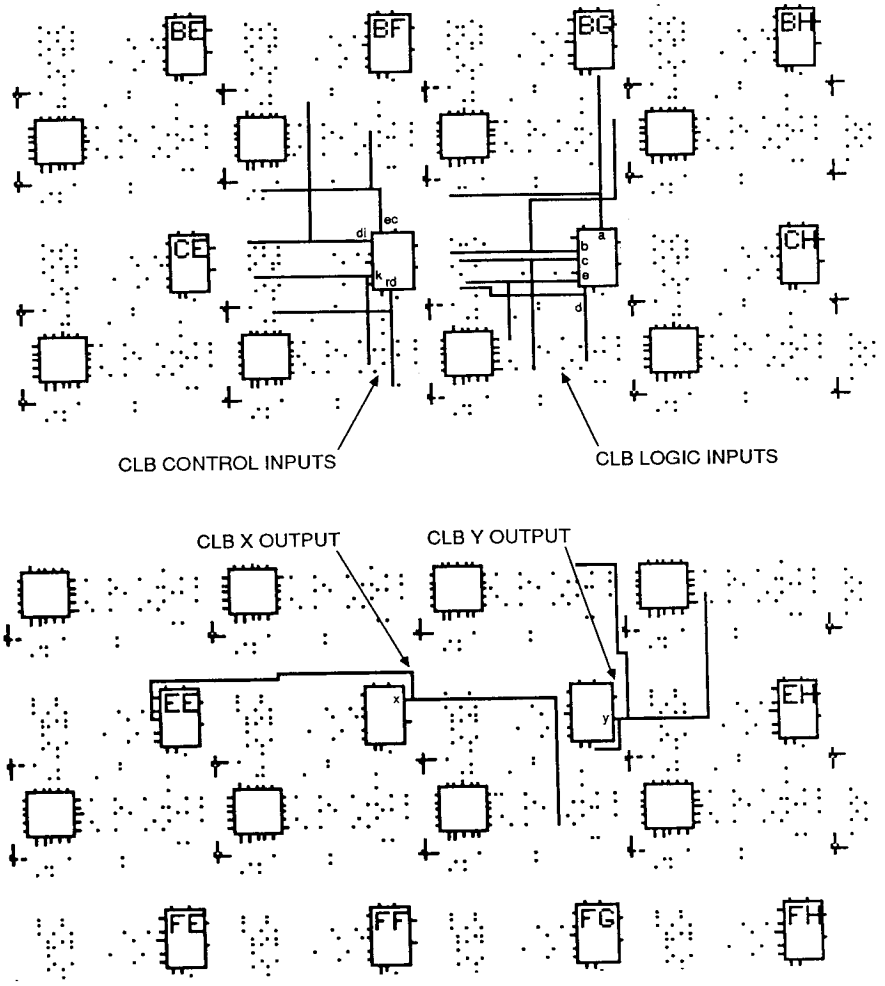

Figure 8. The Xilinx XACT Development System view of the locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect "PIPs" are directional. This is indicated on the XACT design editor status line:

ND is a nondirectional interconnection.
D:H->V is a PIP which drives from a horizontal to a vertical line.
D:V->H is a PIP which drives from a vertical to a horizontal line.
D:C->T is a "T" PIP which drives from a cross of a T to the tail.
D:CW is a corner PIP which drives in the clockwise direction.
P0 indicates the PIP is non-conducting , P1 is "on."

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matricies, above and to the right and may be highlighted by the use of the "Show BIDI" command in XACT. The other PIPs adjacent to the matrices are access to or from long lines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACT development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an XACT option.

Direct Interconnect

Direct interconnect, shown in Figure 11, provides the most efficient implementation of networks between adjacent logic or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each Configurable Logic Block, the *.x* output may be connected directly to the *.b* input of the CLB immediately to its right and to the *.c* input of the CLB to its left. The *.y* output can use direct interconnect to drive the *.d* input of

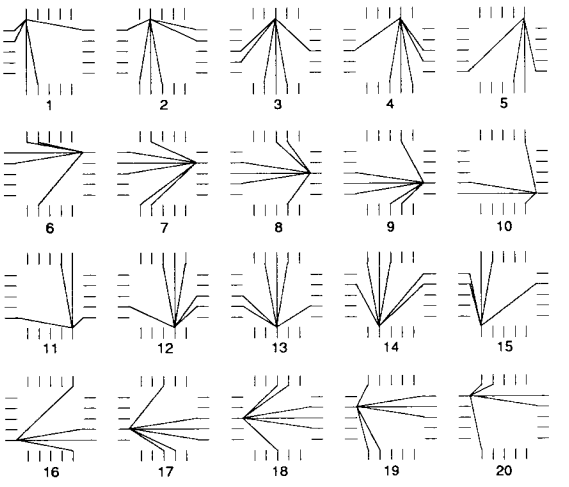

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Figure 10. Switch matrix interconnection options for each "pin." Switch matrices on the edges are different. Use "Show Matrix" menu option in XACT

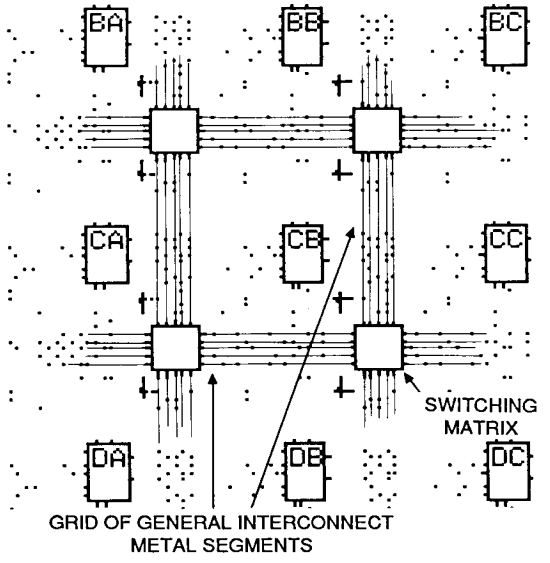


Figure 9. Logic Cell Array general-purpose interconnect is composed of a grid of metal segments which may be interconnected through switch matrices to form networks for CLB and I/O block inputs and outputs.

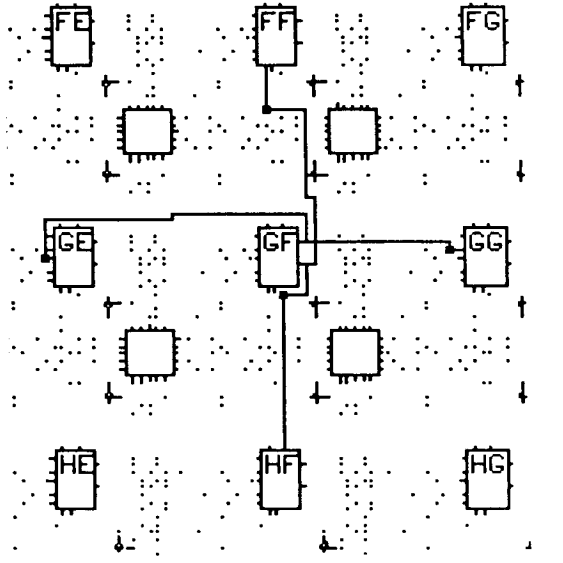


Figure 11. The .x and .y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs.

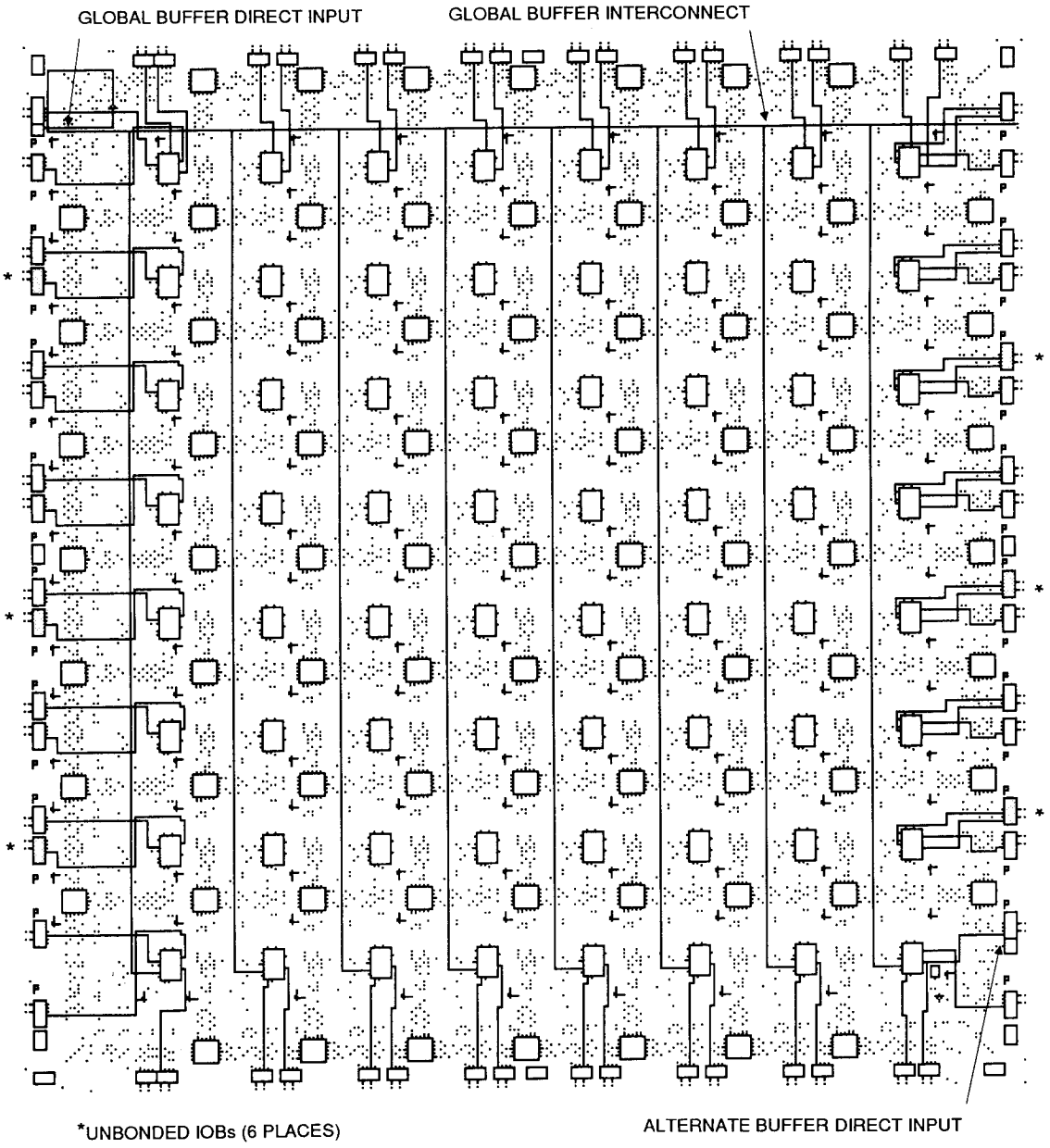


Figure 12. X3020 die edge I/O blocks are provided with direct access to adjacent CLBs.

the block immediately above and the *.a* input of the block below. Direct interconnect should be used to maximize the speed of high performance portions of logic. Where logic blocks are adjacent to I/O Blocks, direct connect is provided alternately to the I/O Block inputs [*.i*] and outputs [*.o*] on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of I/O Blocks with CLBs are shown in Figure 12.

Long Lines

The long lines bypass the switch matrices and are intended primarily for signals which must travel a long distance, or must have minimum skew among multiple destinations. Long Lines, shown in Figure 13, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. An additional two long lines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020, two vertical long lines in each column are connectible half-length lines. On the XC3020 only the outer long lines are.

Long lines can be driven by a logic block or I/O block output on a column by column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in Figure 14. Isolation buffers are provided at each input to a long line and are enabled automatically by the development system when a connection is made.

A buffer in the upper left corner of the Logic Cell Array chip drives a global net which is available to all *.k* inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the I/O and logic blocks. Configuration bits for the *.k* input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for I/O Block use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line that can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the *.k* inputs of the logic blocks. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of three-state buffers is located adjacent to each configurable logic block. These buffers allow logic to drive the horizontal long lines. Logical operation of the three-state buffer controls allows them to implement wide multiplexing functions. Any three-state buffer input can be selected as drive for the horizontal long line bus by applying a low logic level on its three-state control line. See Figure 15a. The user is required to avoid contention which can result from multiple drivers with opposing logic

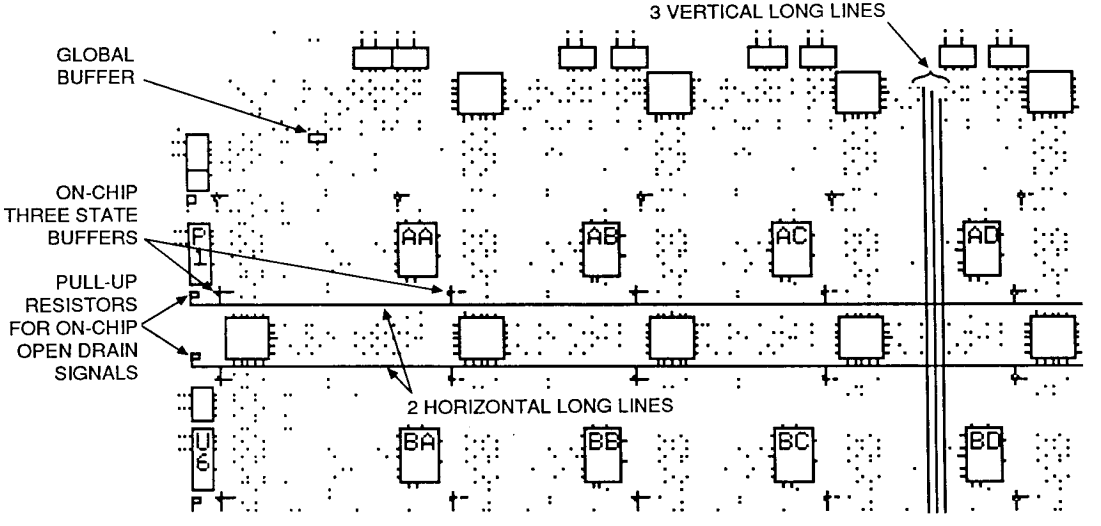


Figure 13. Horizontal and vertical long lines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the LCA.

levels. Control of the three-state input by the same signal that drives the buffer input, creates an 'open drain' wired-AND function. A logical HIGH on both buffer inputs creates a high impedance which represents no contention. A logical LOW enables the buffer to drive the long line low. See Figure 15b. Pull-up resistors are available at each end of the long line to provide a HIGH output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the three-state control lines, these buffers form multiplexers (three-state buses). In this case care must be used to prevent contention through multiple active

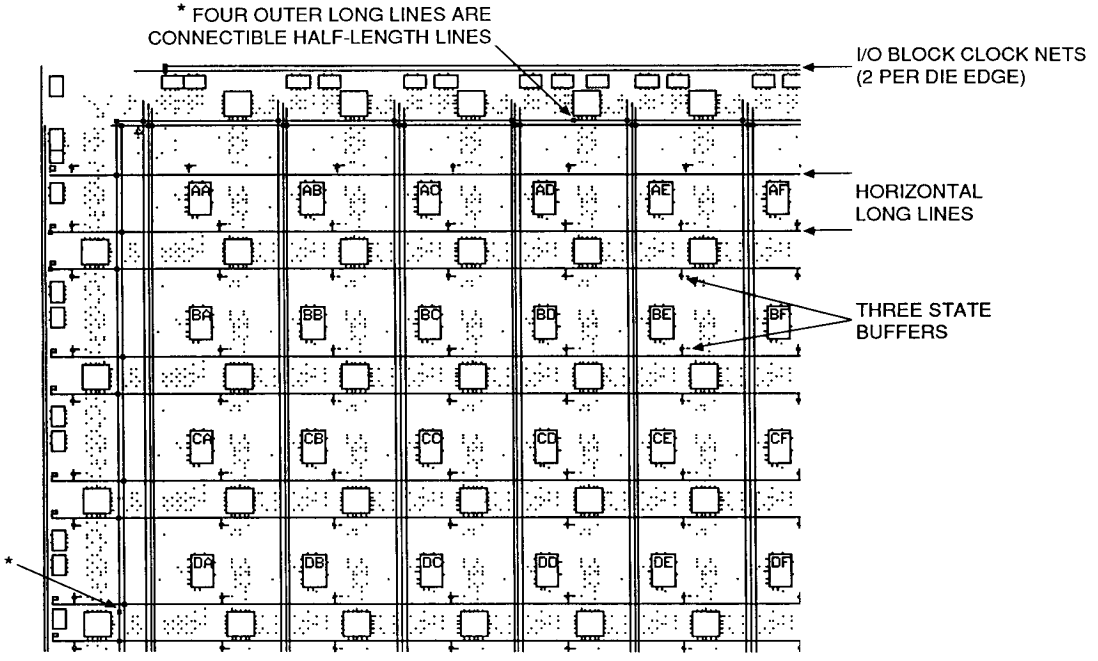


Figure 14. Programmable interconnection of long lines is provided at the edges of the routing area. Three-state buffers allow the use of horizontal long lines to form on-chip wired-AND and multiplexed buses. The left two vertical long lines per column (except 3020) and the outer perimeter long lines may be programmed as connectible half-length.

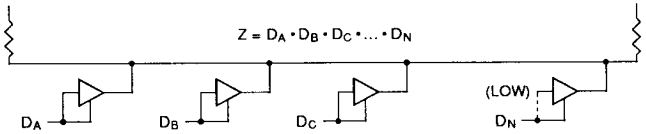
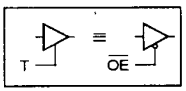


Figure 15a. Three-state buffers implement a Wired-AND function. When all the buffer three state lines are HIGH, (high impedance), the pull-up resistor(s) provide the HIGH output. The buffer inputs are driven by the control signals or a LOW.



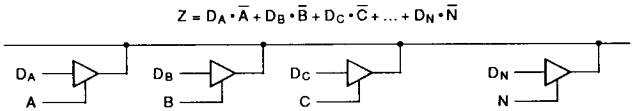


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Figure 15b. Three-state buffers implement a Multiplexer where the selection is accomplished by the buffer three-state signal.

buffers of conflicting levels on a common line. Figure 16 shows three state buffers, long lines and pull-up resistors.

Crystal Oscillator

Figure 16 also shows the location of an internal high speed inverting amplifier which may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by "MAKEBITS" and connected as a signal source, two special user I/O Blocks are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 17. A divide by two option is available to assure symmetry. The oscillator circuit becomes active before configuration is complete in order to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 17 the feedback resistor, R1, between output and input biases the amplifier at threshold. The value should be as large as practical to minimize loading of the crystal. The inversion of the amplifier, together with the R-C networks and an AT cut series resonant crystal, produce the 360 degree phase shift of the Pierce oscillator. A series resistor, R2, may be included to add to the amplifier output impedance when needed for phase shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to one-half the specified CLB toggle frequency. Use at frequen-

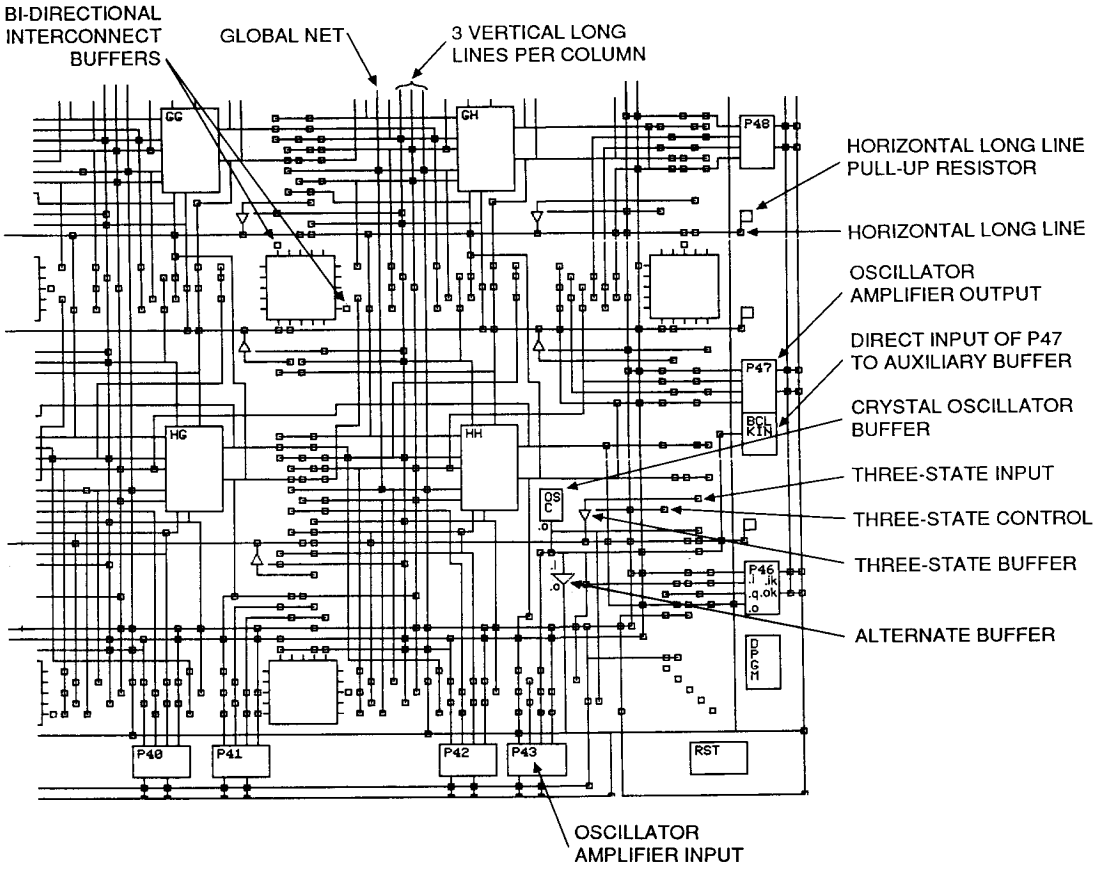


Figure 16. An XACT Development System extra large view of possible interconnections in the lower right corner of the XC3020.

cies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by the R-C networks. When the oscillator inverter is not used, these I/O Blocks and their package pins are available for general user I/O.

PROGRAMMING

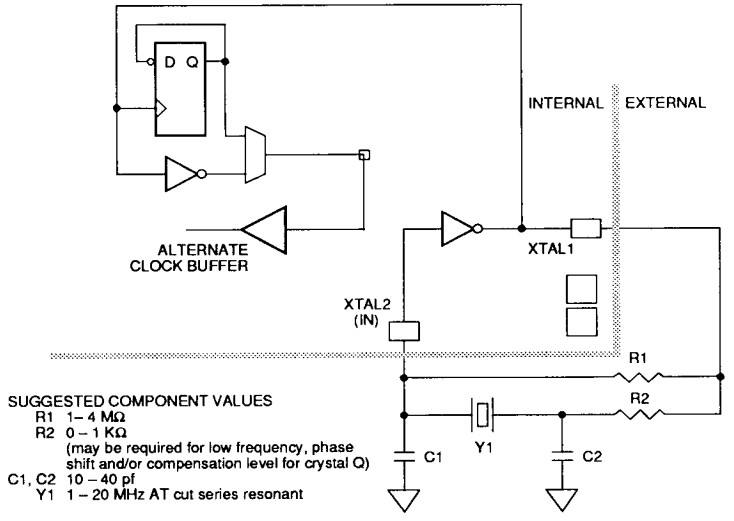
Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When Vcc reaches the voltage at which portions of the LCA begin to operate (2.5 to 3 Volts), the programmable I/O output buffers are disabled and a high impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated, internal timer. This nominal 1 MHz timer is subject to variations with process, temperature and power supply over the range of 0.5 to 1.5 MHz. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

In Master configuration modes the LCA becomes the source of Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An LCA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices which it may be driving will be ready even if the master is very fast, and the slave(s) very slow. Figure 18 shows the state sequences. At the end of Initiali-

Table 1

M0	M1	M2	Clock	Mode	Data
0	0	0	active	Master	Bit Serial
0	0	1	active	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	active	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	passive	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	passive	Slave	Bit Serial



	68 PIN	84 PIN		100 PIN		132 PIN	164 PIN	175 PIN
	PLCC	PLCC	PGA	CQFP	PQFP	PGA	CQFP	PGA
XTAL 1 (OUT)	47	57	J11	67	82	P13	105	T14
XTAL 2 (IN)	43	53	L11	61	76	M13	99	P15

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Figure 17. When activated in the "MAKEBITS" program and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

zation the LCA enters the Clear state where it clears the configuration memory. The active low, open-drain initialization signal $\overline{INIT}$ indicates when the Initialization and Clear states are complete. The LCA tests for the absence of an external active low $\overline{RESET}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{INIT}$ pins can be used to control configuration by the assertion of the active low $\overline{RESET}$ of a master mode device or to signal a processor that the LCAs are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{RESET}$ for a minimum of three internal timer cycles will be recognized and the LCA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The LCA will then re-sample $\overline{RESET}$ and the mode lines before re-entering the Configuration state. A reprogram is initiated when a configured LCA senses a HIGH to LOW transition on the DONE/$\overline{PROG}$ package pin. The LCA returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Logic Cell Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the MakePROM program of the XACT development system begins with a preamble of 111111110010 followed by a 24-bit 'length count' representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 19. All LCAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. An LCA which has received the preamble and length count then presents a HIGH Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an LCA is full and the length count does not compare, the LCA shifts any additional data through, as it did for preamble and length count.

When the LCA configuration memory is full and the length count compares, the LCA will execute a synchronous start-up sequence and become operational. See Figure 20. Three CCLK cycles after the completion of loading configuration data the user I/O pins are enabled as configured. As selected in MAKEBITS, the internal user-logic reset is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/$\overline{PROG}$ output signal. DONE/$\overline{PROG}$ may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDing. The High During Configuration (HDC) and Low During Configuration (LDC) are two user I/O pins which are driven active when an LCA is in its Initialization, Clear or Configure states. They and DONE/$\overline{PROG}$ provide signals for control of external logic signals such as reset, bus enable or PROM enable during configuration. For parallel Master configuration modes these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds

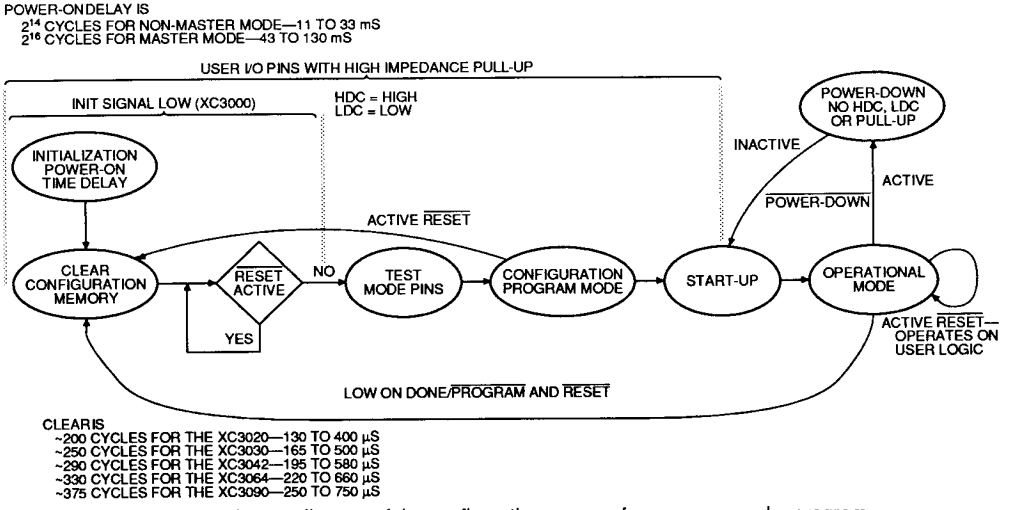


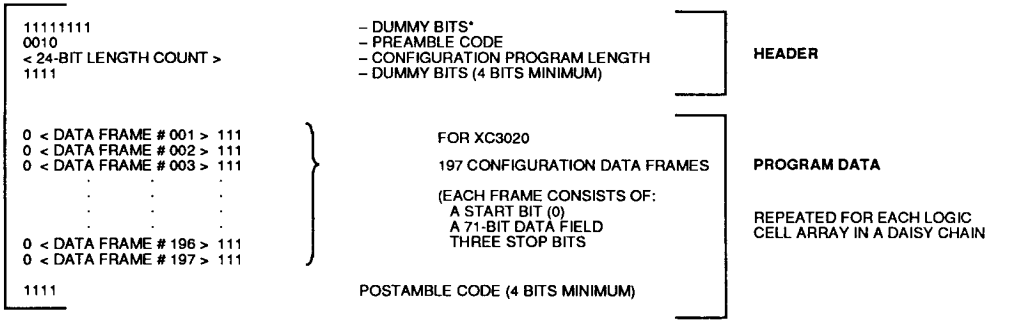
Figure 18. A state diagram of the configuration process for power-up and reprogram.

at the completion of configuration if the user has selected CMOS thresholds. The threshold of $\overline{\text{PWRDWN}}$ and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration Data

Configuration data to define the function and interconnection within a Logic Cell Array are loaded from an external storage at power-up and on a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode se-



*THE LCA DEVICES REQUIRE 4 DUMMY BITS MIN., XACT 2.10 GENERATES 8 DUMMY BITS

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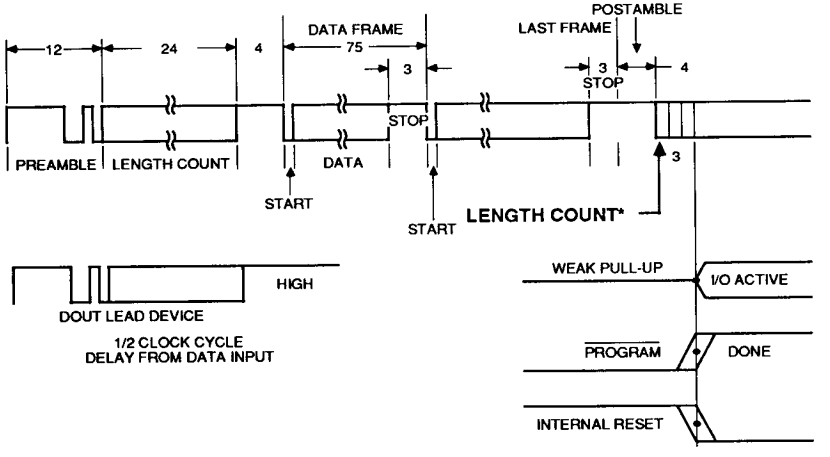
Device	XC3020	XC3030	XC3042	XC3064	XC3090
Gates	2000	3000	4200	6400	9000
CLBs Row X Col	64 (8 X 8)	100 (10 X 10)	144 (12 X 12)	224 (16 X 14)	320 (20 X 16)
IOBs	64	80	96	120	144
Flip-flops	256	360	480	688	928
Bits per frame (w/ 1 start 3 stop)	75	92	108	140	172
Frames	197	241	285	329	373
Program Data = Bits * Frames + 4 (excludes header)	14779	22176	30784	46064	64160
PROM size (bits) = Program Data + 40 bit Headers	14819	22216	30824	46104	64200

Figure 19. The internal Configuration Data Structure for an LCA shows the preamble, length count and data frames which are generated by the XACT Development System.

The Length Count produced by the "MAKEBIT" program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \leq K \leq 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

lection pins at the start of configuration time determine the method to be used. See Table 1. The data may be either bit-serial or byte-parallel, depending on the configuration mode. Various Xilinx Programmable Gate Arrays have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx 2000 and 3000 product families use compatible configuration formats. For the XC3020, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See Figure 20. The specific data format for each device is produced by the MAKEBITS command of the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the 'MAKE PROM' command of the XACT development system. A compatibility exception precludes the use of a 2000 series device as the master for 3000 series devices if their DONE or RESET are programmed to occur after their outputs become active. The "tie" option of the MAKEBITS program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminant levels which might produce parasitic supply currents. If unused blocks are not sufficient to complete the 'tie,' the FLAGNET command of EDITLCA can be used to indicate nets which must not be used to drive the remaining unused routing, as that might affect timing of user nets. NORESTORE will retain the results of TIE for timing analysis with QUERYNET before RESTORE returns the design to the untied condition. TIE can be omitted for quick breadboard iterations where a few additional mA of Icc are acceptable.

The configuration bit-stream begins with HIGH preamble bits, a four-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the LCA is set to 0 and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the LCA, it is internally assembled into a data word. As each data word is completely assembled, it is loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held reset during configuration.



* THE CONFIGURATION DATA CONSISTS OF A COMPOSITE 40-BIT PREAMBLE/LENGTH-COUNT, FOLLOWED BY ONE OR MORE CONCATENATED LCA PROGRAMS, SEPARATED BY 4-BIT POSTAMBLES. AN ADDITIONAL FINAL POSTAMBLE BIT IS ADDED FOR EACH SLAVE DEVICE AND THE RESULT ROUNDED UP TO A BYTE BOUNDRY. THE LENGTH COUNT IS TWO LESS THAN THE NUMBER OF RESULTING BITS.

TIMING OF THE ASSERTION OF DONE AND TERMINATION OF THE INTERNAL RESET MAY EACH BE PROGRAMMED TO OCCUR ONE CYCLE BEFORE OR AFTER THE I/O OUTPUTS BECOME ACTIVE.

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Figure 20. Configuration and start-up of one or more LCAs.

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Two user programmable pins are defined in the unconfigured Logic Cell array. High During Configuration (HDC) and Low During Configuration (LDC) as well as DONE/$\overline{PROG}$ may be used as external control signals during configuration. In Master mode configurations it is convenient to use LDC as an active-low EPROM Chip Enable. After the last configuration data-bit is loaded and the length count compares, the user I/O pins become active. Options in the MAKEBITS program allow timing choices of one clock earlier or later for the timing of the end of the internal logic reset and the assertion of the DONE signal. The open-drain DONE/$\overline{PROG}$ output can be AND-tied with multiple Logic Cell Arrays and used as an active high READY, an active low PROM enable or a RESET to other portions of the system. The state diagram of Figure 18 illustrates the configuration process.

Master Mode

In Master mode, the Logic Cell Array automatically loads configuration data from an external memory device. There are three Master modes which use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Serial Master mode uses serial configuration data supplied to data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 21. Parallel Master Low and Master High modes automatically use parallel data sup-

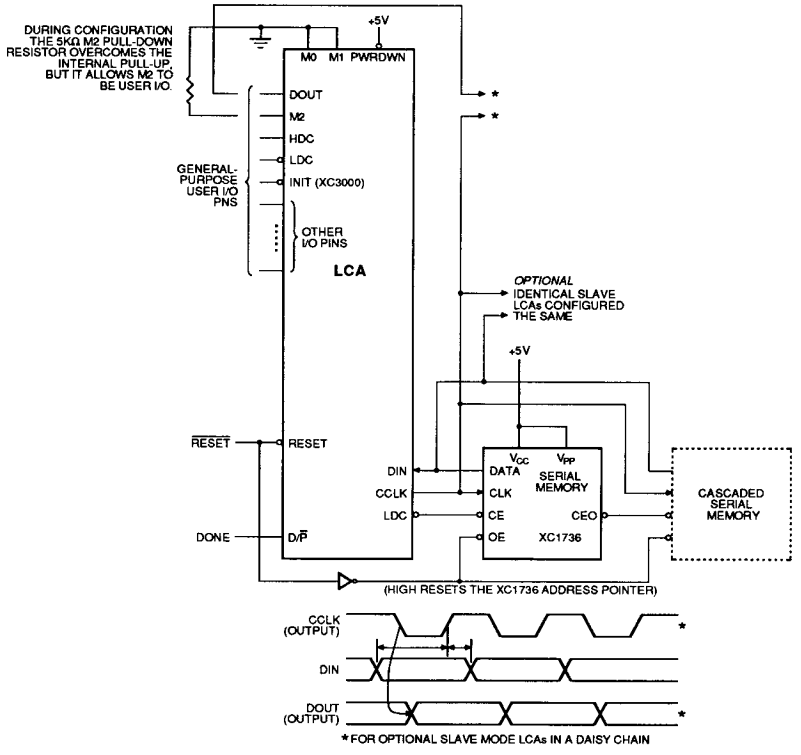

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Figure 21. Master Serial Mode. The one-time-programmable XC1736 Serial Configuration PROM supports automatic loading of configuration programs up to 36K bits. Multiple devices can be cascaded to support additional LCAs. An early DONE inhibits the XC1736 data output a $\overline{CCLK}$ cycle before the LCA I/O become active.

plied to the D0–D7 pins in response to the 16-bit address generated by the LCA. Figure 22 shows an example of the parallel Master mode connections required. The LCA HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory. For Master high or low, data bytes are read in parallel by each read clock (RCLK) and internally serialized by the configuration clock. As each data byte is read, the least significant bit of the next byte, D0, becomes the next bit in the internal serial configuration word. One Master mode LCA can be used to interface the configuration program-store and pass additional concatenated configuration data to additional LCAs in a serial daisy-chain fashion. CCLK is provided for the slaved devices and their serialized data is supplied from DOUT to DIN - DOUT to DIN etc.

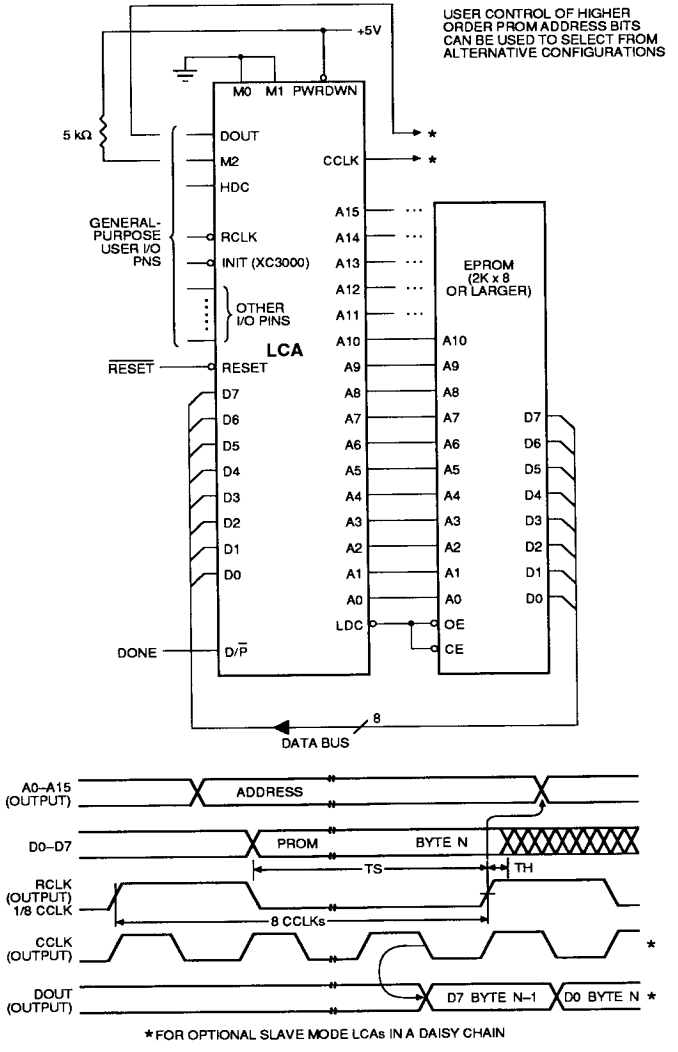

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Figure 22. Master Parallel Mode. Configuration data are loaded automatically from an external byte wide PROM. An early DONE inhibits the PROM outputs a CCLK before the LCA I/O become active.

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 23 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe ($\overline{WS}$), and two active low and one active high Chip Selects ($\overline{CS0}$, $\overline{CS1}$, CS2). If all these signals are not available, the unused inputs should be driven to their respective active levels. The Logic Cell Array will accept one byte of configuration data on the D0–D7 inputs for each selected processor Write cycle. Each byte of data is loaded into a buffer register. The LCA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output HIGH on READY/$\overline{BUSY}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Mode

Slave mode provides a simple interface for loading the Logic Cell Array configuration as shown in Figure 24. Serial data are supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input are supplied by the previous Logic Cell Array's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy-Chain

The Xilinx XACT development system is used to create a composite configuration bit stream for selected LCAs

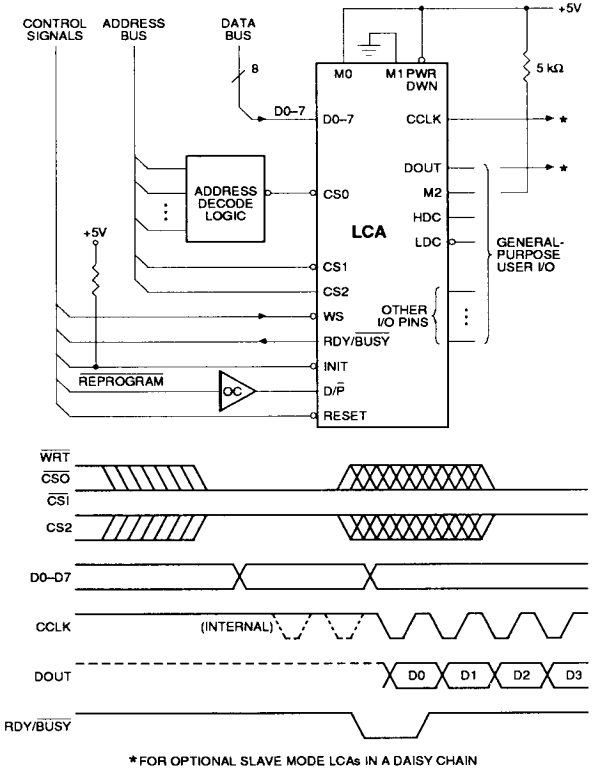

Figure 23. Peripheral Mode. Configuration data are loaded using a byte-wide data bus from a microprocessor.

including: a preamble, a length count for the total bit-stream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a HIGH DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data are passed through the lead device and appear on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream LCAs. Data are read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

Special Configuration Functions

The configuration data include control over several special functions in addition to the normal user logic functions and interconnect:

- Input thresholds
- Readback enable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal XACT development system bit-stream generation process.

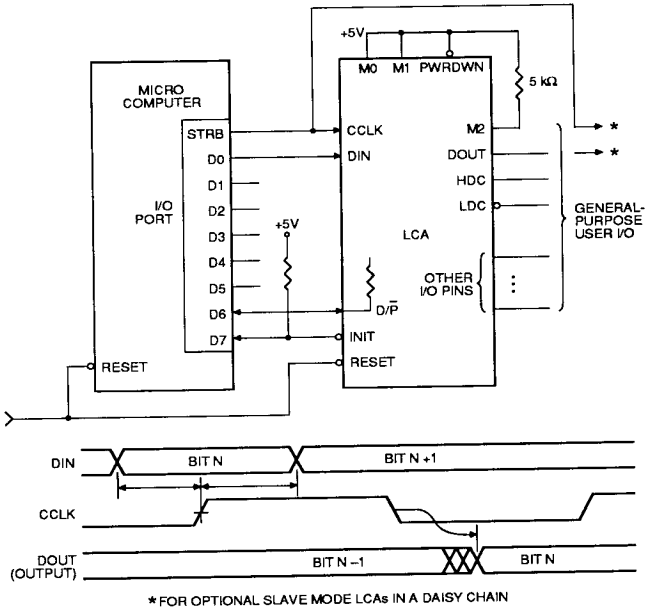

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Figure 24. Slave Mode. Bit-serial configuration data are read at rising edge of the CCLK. Data on DOUT are provided on the falling edge of CCLK.

Input Thresholds

Prior to the completion of configuration all LCA input thresholds are TTL compatible. Upon completion of configuration the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the $\overline{\text{PWRDWN}}$ input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the I/O Block pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Logic Cell Array may be read back if it has been programmed with a bit-stream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging with the XACTOR In-Circuit debugger. There are three options in generating the configuration bit-stream:

- "Never" will inhibit the Readback capability.
- "One-time," will inhibit Readback after one Readback has been executed to verify the configuration.
- "On-command" will allow unrestricted use of Readback.

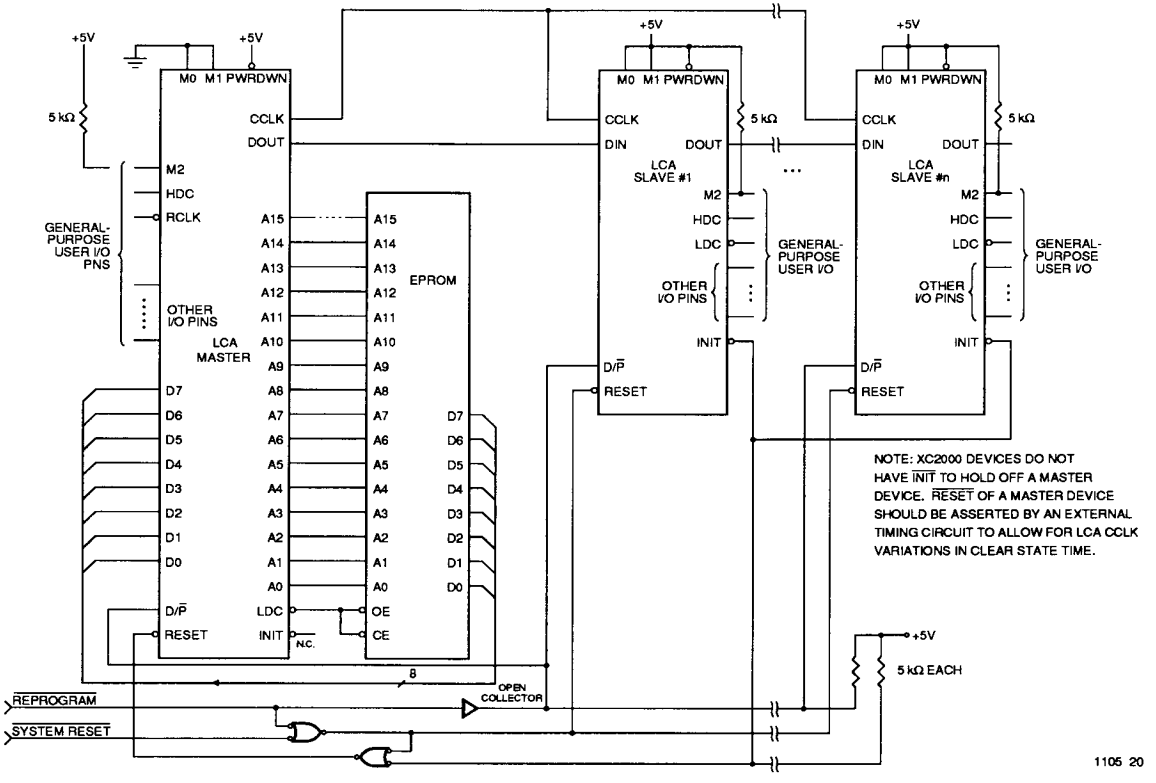


Figure 25. Master Mode configuration with daisy chained slave mode devices. All are configured from the common EPROM source. The Slave mode device $\overline{\text{INIT}}$ signals delay the Master device configuration until they are initialized. A well defined termination of SYSTEM RESET is needed when controlling multiple LCAs.

Any XC3000 slave driven by an XC2000 master mode device must use "early DONE and early internal reset". (The XC2000 master will not supply the extra clock required by a "late" programmed XC3000.)

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of readback is produced by a LOW to HIGH transition of the M0/RTRIG (Read Trigger) pin. Once the readback command has been given, the input CCLK is driven by external logic to read back each data bit in a format similar to loading. After two dummy bits, the first data frame is shifted out, in inverted sense, on the M1/$\overline{\text{RDATA}}$ (Read Data) pin. All data frames must be read back to complete the process and return the mode select and CCLK pins to their normal functions.

The readback data includes the current state of each internal logic block storage element, and the state of the [*.i* and *.ri*] connection pins on each I/O Block. These data are imbedded into unused configuration bit positions during readback. This state information is used by the Logic Cell Array development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements it may be necessary to inhibit the system clock.

Re-program

The Logic Cell Array configuration memory can re-written while the device is operating in the user's system. To initiate a re-programming cycle, the dual function package pin DONE/$\overline{\text{PROG}}$ must be given a HIGH to LOW transition. To reduce sensitivity to noise, the input signal is filtered for 2 cycles of the LCA's internal timing generator. When re-program begins, the user programmable I/O output buffers are disabled and high impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates 'initialized'. Since this clear operation uses chip-individual internal timing, the master might complete the clear operation and then start configuration before the slave has completed the clear operation. To avoid this problem, wire-AND the slave $\overline{\text{INIT}}$ pins and use them to force a RESET on the master (see Figure 25). Reprogram control is often implemented using an external open collector driver which pulls DONE/$\overline{\text{PROG}}$ LOW. Once it recognizes a stable request, the Logic Cell Array will hold a LOW until the new configuration has been completed. Even if the re-program request is externally held LOW beyond the configuration period, the Logic Cell Array will begin operation upon completion of configuration.

DONE Pull-up

DONE/$\overline{\text{PROG}}$ is an open drain I/O pin that indicates the LCA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the XACT development system when 'Make Bits' is executed. The DONE/$\overline{\text{PROG}}$ pins of multiple LCAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to re-program.

DONE Timing

The timing of the DONE status signal can be controlled by a selection in the MAKEBITS program to occur a CCLK cycle before, or after, the timing of outputs being activated. See Figure 20. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal RESET can be controlled by a selection in the MAKEBITS program to occur a CCLK cycle before, or after, the timing of outputs being enabled. See Figure 20. This reset maintains all user programmable flip-flops and latches in a 'zero' state during configuration.

Crystal Oscillator Division

A selection in the MAKEBITS program allows the user to incorporate a dedicated divide-by-two flip-flop in the crystal oscillator function. This provides higher assurance of a symmetrical timing signal. Although the frequency stability of crystal oscillators is high, the symmetry of the waveform can be affected by bias or feedback drive.

PERFORMANCE

Device Performance

The high performance of the Logic Cell Array is due in part to the manufacturing process, which is similar to that used for high speed CMOS static memories. Performance can be measured in terms of minimum propagation times for logic elements. The parameter which traditionally describes the overall performance of a gate array is the toggle frequency of a flip-flop. The configuration for determining the toggle performance of the Logic Cell Array is shown in Figure 26. The flip-flop output Q is fed back through the combinatorial logic as $\overline{Q}$ to form the toggle flip-flop.

Actual Logic Cell Array performance is determined by the timing of critical paths, including both the fixed timing for the logic and storage elements in that path, and the timing associated with the routing of the network. Examples of internal worst case timing are included in the performance data to allow the user to make the best use of the capabilities of the device. The XACT development system timing calculator or XACT generated simulation models should be used to calculate worst case paths by using actual impedance and loading information. Figure 27 shows a variety of elements which are involved in determing system performance. Actual measurement of internal timing is not practical and often only the sum of component timing is relevant as in the case of input to output. The relationship between input and output timing is arbitrary and only the total determines performance. Timing components of internal functions may be determined by measurement of differences at the pins of the package. A synchronous logic function which involves a clock to block-output, and a block-input to clock set-up is capable of higher speed operation than a logic configuration of two synchronous blocks with an extra combinatorial block level between them. System clock rates to 60% of the toggle frequency are practical for logic in which an extra combinatorial level is located between synchronized blocks. This allows implementation of functions of up to 25 variables. The use of the wired-AND is also available for wide, high speed functions.

Logic Block Performance

Logic block performance is expressed as the propagation time from the interconnect point at the input of the combinatorial logic to the output of the block in the interconnect area. Combinatorial performance is independent of the specific logic function because of the table look-up based implementation. Timing is different when the combinatorial logic is used in conjunction with the storage element. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing of signals produced by storage elements. Loading of a Logic Block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See Figures 28 and 29.

Interconnect Performance

Interconnect performance depends on the routing resource used to implement the signal path. As discussed earlier, direct interconnect from block to block provides a fast path for a signal. The single metal segment used for Long lines exhibits low resistance from end to end, but relatively high capacitance. Signals driven through a programmable switch will have the additional impedance of the switch added to their normal drive impedance.

General purpose interconnect performance depends on the number of switches and segments used, the presence of the bi-directional re-powering buffers and the overall loading on the signal path at all points along the path. In calculating the worst case timing for a general interconnect path the timing calculator portion of the XACT development system accounts for all of these elements. As an approximation, interconnect timing is proportional to the summation of totals of local metal segments beyond each programmable switch. In effect, the time is a sum of R-C time each approximated by an R times the total C it drives. The R of the switch and the C of the interconnect is a function of the particular device performance grade. For a string of three local interconnects, the approximate time at the first segment, after the first switch resistance would be three units; an additional two units after the next switch plus an additional unit after the last switch in the chain. The interconnect R-C chain terminates at each re-powering buffer. The capacitance of the actual block inputs is not significant; the capacitance is in the interconnect metal and switches. Figure 30 illustrates this.

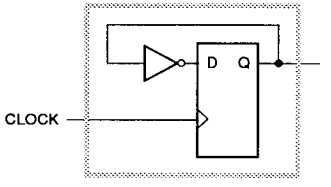
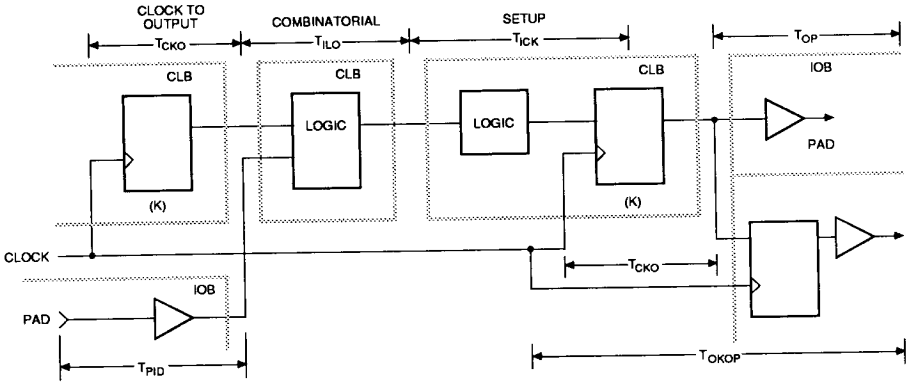


Figure 26. "Toggle" Flip-Flop used to characterize device performance.



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		Speed Grade	-50		-70		-100		Units
	Description	Symbol	Min	Max	Min	Max	Min	Max	
Logic input to Output	Combinatorial	T_{ILO}		14		9		7	ns
K Clock	To output	T_{CKO}		12		8		7	ns
	Logic-input setup	T_{ICK}	12		8		7		ns
	Logic-input hold	T_{CKI}	0		0		0		ns
Input/Output	Pad to input (direct)	T_{PID}		9		6		4	ns
	Output to pad (fast)	T_{OP}		15		9		6	ns
	I/O clock to pad (fast)	T_{OKPO}		18		13		10	ns
FF toggle frequency		F_{CLK}		50		70		100	MHz

Figure 27. Examples of Primary Block Speed Factors.
Actual timing is a function of various block factors combined with routing factors.
Overall performance can be evaluated with the XACT timing calculator or by an optional simulation.

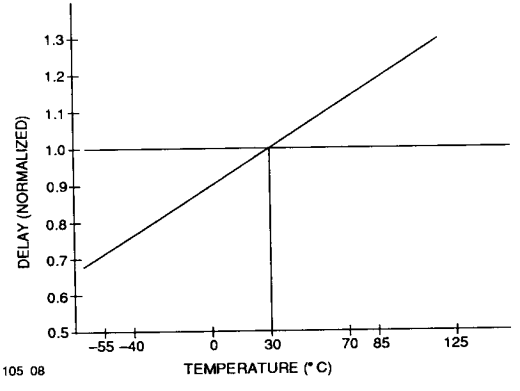

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Figure 28. Change in speed performance as a function of temperature, normalized for 30°C.

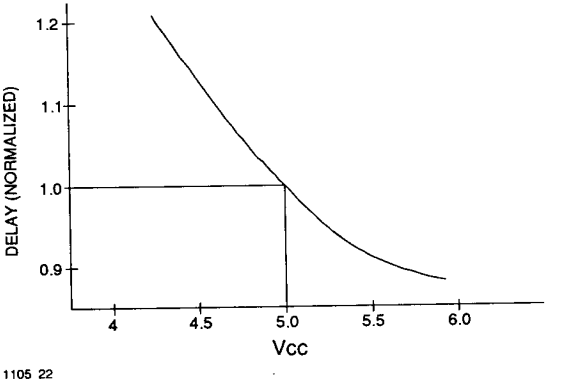

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Figure 29. The speed performance of a CMOS device increases with Vcc within the operating range.

POWER

Power Distribution

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, a dedicated Vcc and ground ring surrounding the logic array provides power to the I/O drivers. See Figure 31. An independent matrix of Vcc and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1 µF capacitor connected near the Vcc and ground pins of the package will provide adequate decoupling.

Output buffers capable of driving the specified 4 mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their DC drive capability, but generate less external reflections and internal noise. More than 32 fast outputs should not be switching in the same direction exactly simultaneously. A few ns of deliberate skew can alleviate this problem of "ground-bounce".

Power Dissipation

The Logic Cell Array exhibits the low power consumption characteristic of CMOS ICs. For any design the user can use Figure 32 to calculate the total power requirement based on the sum of the capacitive and DC loads both external and internal. The configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells which hold the configuration data is very low and may be maintained in a power-down mode.

Typically most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the DC loading on each output pin by devices driven by the Logic Cell Array.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an LCA the fraction of nodes changing on a given clock is typically low (10–20%). For example, in a large binary counter, the average clock cycle produces changes equal to one CLB output at the clock frequency. Typical global clock buffer power is between 1.7 mW/MHz for the XC3020 and 3.6 mW/MHz for the XC3090. The internal capacitive load is more a function of interconnect than fan-out. With a "typical" load of three general interconnect segments, each Configurable Logic Block output requires about 0.4 mW per MHz of its output frequency.

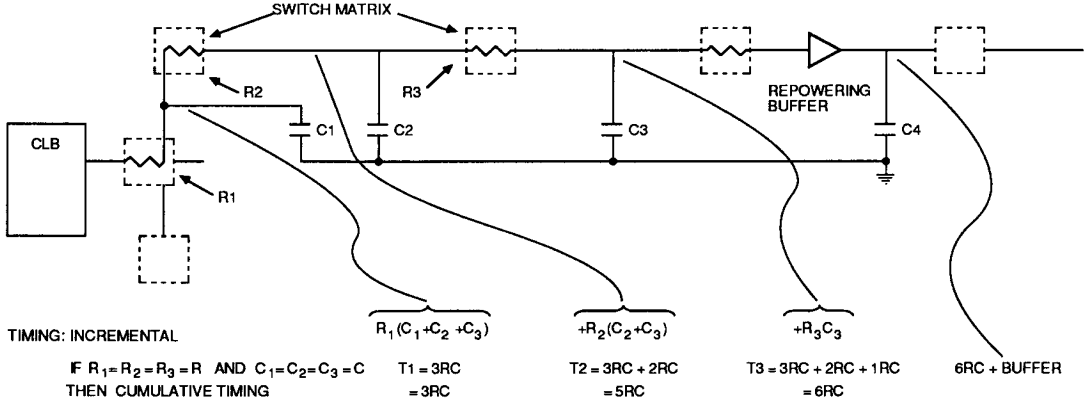

Figure 30. Interconection timing example. Use of the XACT timing calculator or XACT-generated simulation model provide actual worst-case performance information.

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Total Power = Vcc • Icco + external (DC + capacitive)
+ internal (CLB + IOB + Long Line + pull-up)

Because the control storage of the Logic Cell Array is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The Logic Cell Array has built in power-down logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high impedance state with no pull-ups. Power-down data retention is possible with a simple battery-backup circuit because the power requirement is extremely low. For retention at 2.4 volts the required current is typically on the order of 50 nanoamps.

To force the Logic Cell Array into the Power-Down state, the user must pull the $\overline{\text{PWRDWN}}$ pin low and continue to supply a retention voltage to the Vcc pins of the package. When normal power is restored, Vcc is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a HIGH. The Logic Cell Array resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal I/O and logic block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released. No configuration programming is involved.

When the power supply is removed from a CMOS device it is possible to supply some power from an input signal. The conventional electro-static input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the power pin. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bi-polar buffer may be used to isolate the input signal.

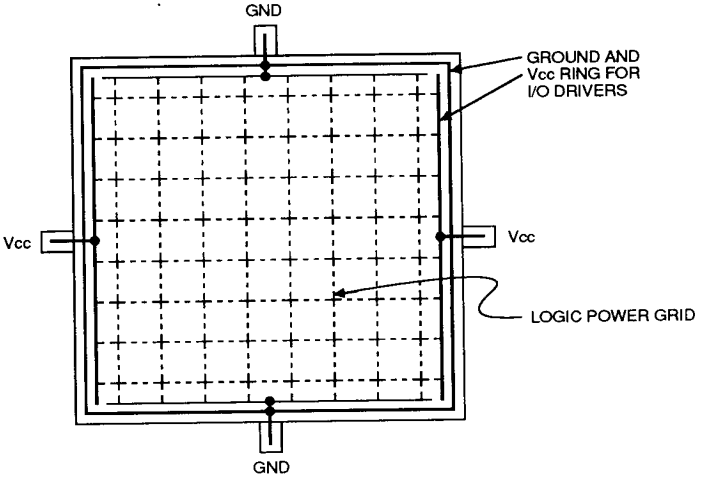

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Figure 31. LCA Power Distribution.

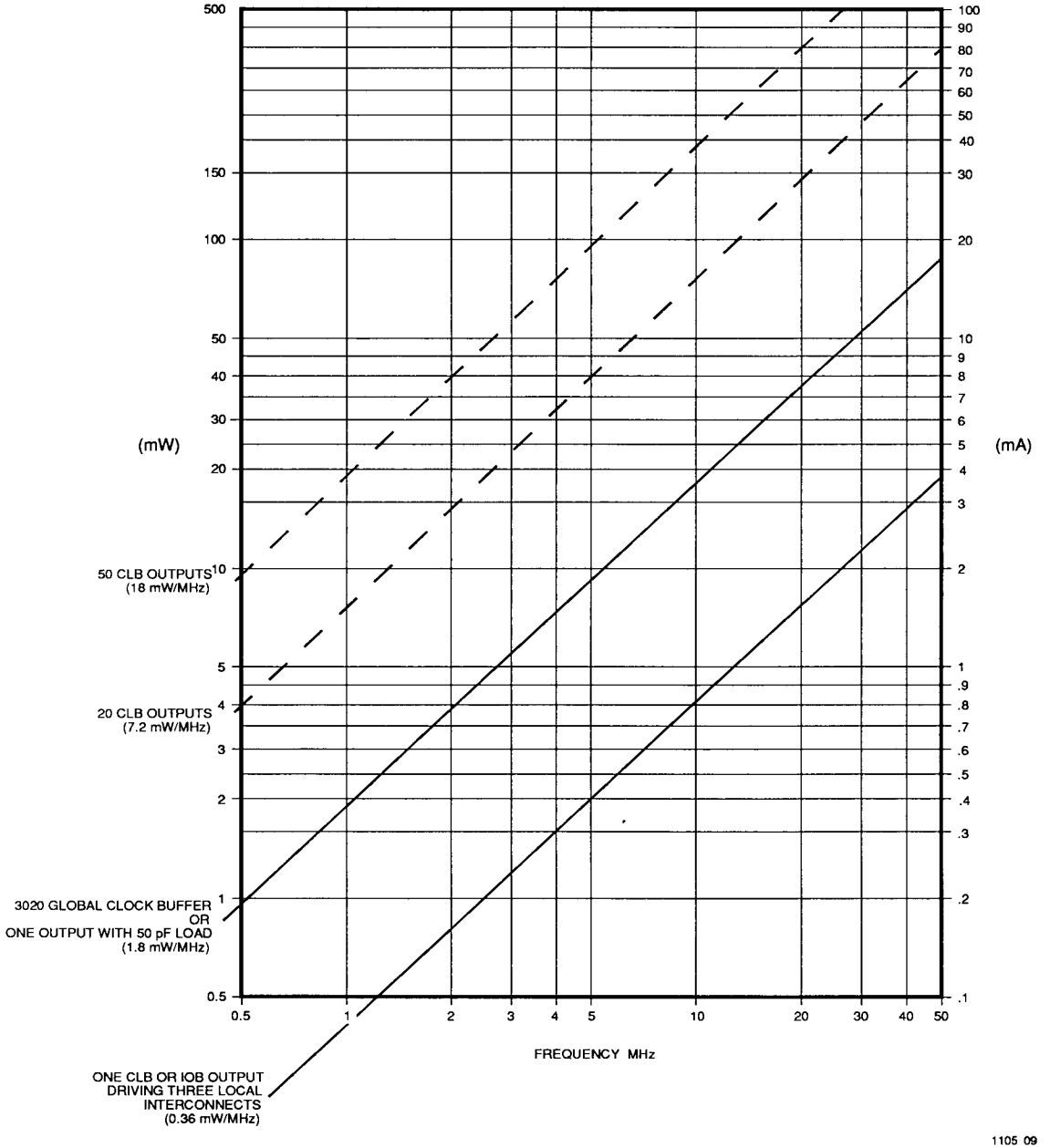

Figure 32. LCA Power Consumption by Element. Total chip power is the sum of Vcc•Icco plus effective internal and external values of frequency dependent capacitive charging currents and duty factor dependent resistive loads.

Component Selection, Ordering Information, Electrical Parameters & Physical Dimensions

		48 PIN		68 PIN		84 PIN		100 PIN		132 PIN		164 PIN	175 PIN	
		PLASTIC DIP	CERAMIC DIP	PLASTIC PLCC	CERAMIC PGA	PLASTIC PLCC	CERAMIC PGA	PLASTIC PQFP	CERAMIC CQFP	PLASTIC PGA	CERAMIC PGA	CERAMIC CQFP	PLASTIC PGA	CERAMIC PGA
		-PD48	-CD48	-PC68	-PG68	-PC84	-PG84	-PQ100	-CQ100	-PP132	-PG132	-CQ164	-PP175	-PG175
XC2064	-33	C	I M	C I	C I M									
	-50	C	I	C I	C I M									
	-70			C I	C I M									
	-100			C	C									
XC2018	-33			C I		C I	C I M B							
	-50			C I		C I	C I M B							
	-70			C I		C I	C I M							
	-100			C		C	C							
XC3020	-50			C I		C I	C I M B	C I	C I M B					
	-70			C I		C I	C I M	C I	C I M					
	-100			C		C	C	C	C					
XC3030	-50			C I		C I	C I M	C I	C I M					
	-70			C I		C I	C I M	C I	C I M					
	-100			C		C	C	C	C					
XC3042	-50					C I	C I M	C I	C I M	C I	C I M B			
	-70					C I	C I M	C I	C I M	C I	C I			
	-100					C	C	C	C	C	C			
XC3064	-50									C I	C I M			
	-70									C I	C I			
	-100									C	C			
XC3090	-50											C I M	C I	C I M B
	-70											C I M	C I	C I M
	-100											C	C	C

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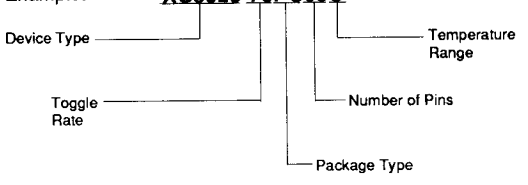
XC1736-PD8C **Plastic 8 Pin, Mini-DIP** **–40°C to 85°C**
XC1736-CD8M **Ceramic 8 Pin, Mini-DIP** **–55°C to 125°C**

LCA Temperature Options

Symbol	Description	Temperature
C	Commercial	0°C to 70°C
I	Industrial	–40°C to 85°C
M	Military	–55°C to 125°C
B	Military	MIL-STD-883, Class B

ORDERING INFORMATION

Example: **XC3020-70PC68C**



COMPATIBLE PACKAGE OPTIONS

A range of Xilinx LCA devices is available in identical packages with identical pin-outs. A design can thus be started with one device, then migrated to a larger or smaller chip while retaining the original footprint and PC-board layout.

Examples:	PLCC 68:	2064-2018-3020-3030
	PLCC 84:	2018-3020-3030-3042
	PGA 84:	2018-3020-3030-3042
	PQFP 100:	3020-3030-3042
	CQFP100:	3020-3030-3042
	PGA 132:	3042-3064

Note, however, that the XC2000 and XC3000 families differ in the position of XTL1 as well as three parallel address bits (6, 7 and 11) and most of the data pins used in parallel master mode.

XC2018 and XC3020 are not available in PGA68, since the PGA84 is the same size and offers more I/O.

Note that a PLCC in a socket with PGA footprint generates a printed circuit board pin-out **different** from a PGA device.

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PIN DESCRIPTIONS

1. Permanently Dedicated Pins.

Vcc
Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$
A LOW on this CMOS compatible input stops all internal activity to minimize Vcc power, and puts all output buffers in a high impedance state, but configuration is retained. When the $\overline{\text{PWRDWN}}$ pin returns HIGH, the device returns to operation with the same sequence of buffer enable and DONE/$\overline{\text{PROGRAM}}$ as at the completion of configuration. All internal storage elements are reset. If not used, $\overline{\text{PWRDWN}}$ must be tied to Vcc.

$\overline{\text{RESET}}$
This is an active low input which has three functons.

Prior to the start of configuration, a LOW input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the "M" lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the LCA is re-initialized and will restart the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete it will provide an asynchronous reset of all IOB and CLB storage elements of the LCA.

CCLK
During configuration, Configuration Clock is an output of an LCA in Master mode or Peripheral mode. LCAs in Slave mode use it as a clock input. During a Readback operation it is a clock input for the configuration data being shifted out.

DONE
The DONE output is configurable as open drain with or without an internal pull-up resistor. At the completion of configuration, the circuitry of the LCA becomes active in a synchronous order, and DONE may be programmed to occur one cycle before or after that.

PROG
Once configuration is done, a HIGH to LOW transition of this pin will cause an initialization of the LCA and start a reconfiguration.

M0
As Mode 0, this input and M1, M2 are sampled before the start of configuration to establish the configuration mode to be used.

RTRIG
As a Read Trigger, a LOW-to-HIGH input transition, after configuration is complete, will initiate a Readback of configuration and storage element data by CCLK. This operation may be limited to a single request, or be inhibited altogether, by selecting the appropriate readback option when generating the bit stream.

M1
As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is to be used, a 5 KΩ resistor should be used to define mode level inputs.

$\overline{\text{RDATA}}$
As an active low Read Data, after configuration is complete, this pin is the output of the readback data.

2. User I/O Pins that can have special functions.

M2
As Mode 2 this input has a passive pullup during configuration. Together with M0 and M1 it is sampled before the start of configuration to establish the configuration mode to be used. After configuration this pin becomes a user programmable I/O pin.

HDC
High During Configuration is held at a HIGH level by the LCA until after configuration. It is available as a control output indicating that configuration is not yet completed. After configuration this pin is a user I/O pin.

$\overline{LDC}$
Low During Configuration is held at a LOW level by the LCA until after configuration. It is available as a control output indicating that configuration is not yet completed. It is particularly useful in Master mode as a LOW enable for an EPROM. After configuration this pin is a user I/O pin. If used as a LOW EPROM enable, it must be programmed as a HIGH after configuration.

$\overline{INIT}$
This is an active low open drain output which is held LOW during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user programmable I/O pin.

BCLKIN
This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MAKEBITS program.

$\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WS}$
These four inputs represent a set of signals, three active low and one active high, which are used in the Peripheral mode to control configuration data entry. The assertion of all 4 generates a write to the internal data buffer. The removal of any assertion, clocks in the D0–D7 data present.

$\overline{RCLK}$
During Master parallel mode configuration $\overline{RCLK}$ represents a "read" of an external dynamic memory device (normally not used).

RDY/$\overline{BUSY}$
During Peripheral parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user programmed I/O pin.

D0–D7
This set of 8 pins represent the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete they are user programmed I/O pin.

A0–A15
This set of 16 pins present an address output for a configuration EPROM during Master parallel mode. After configuration is complete they are user programmed I/O pin.

DIN
This user I/O pin is used as serial Data input during Slave or Master Serial configuration. This pin is Data 0 input in Master or Peripheral configuration mode.

DOUT
This user I/O pin is used during configuration to output serial configuration data for daisy-chained slaves' Data In.

TCLKIN
This is a direct CMOS level input to the global clock buffer.

3. Unrestricted User I/O Pins.

I/O
A pin which may be programmed by the user to be Input and/or Output pin following configuration. Some of these pins present a high impedance pull-up (see next page) or perform other functions before configuration is complete (see above).

XC3000 Family Configuration Pin Assignments

CONFIGURATION MODE: <M2:M1:M0>					68 PLCC	84 PLCC	84 PGA	100 PQFP	100 CQFP	132 PGA	164 CQFP	175 PGA	USER OPERATION
SLAVE <1:1:1>	MASTER-SER <0:0:0>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>									
PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	10	12	B2	29	14	A1	20	B2	PWR DWN (I)
VCC	VCC	VCC	VCC	VCC	18	22	F3	41	26	C8	42	D9	VCC
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	25	31	J2	52	37	B13	62	B14	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	26	32	L1	54	39	A14	64	B15	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	27	33	K2	56	41	C13	66	C15	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	28	34	K3	57	42	B14	67	E14	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	30	36	L3	59	44	D14	71	D16	I/O
* INIT	INIT	INIT	INIT	INIT	34	42	K6	65	50	G14	81	H15	I/O
GND	GND	GND	GND	GND	35	43	J6	66	51	H12	83	J14	GND
					43	53	L11	76	61	M13	99	P15	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	44	54	K10	78	63	P14	101	R15	RESET (I)
DONE	DONE	DONE	DONE	DONE	45	55	J10	80	65	N13	103	R14	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	46	56	K11	81	66	M12	104	N13	I/O
					47	57	J11	82	67	P13	105	T14	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	48	58	H10	83	68	N11	109	P12	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	49	60	F10	87	72	M9	115	T11	I/O
		CS0 (I)			50	61	G10	88	73	N9	116	R10	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	51	62	G11	89	74	N8	121	R9	I/O
VCC	VCC	VCC	VCC	VCC	52	64	F9	91	76	M8	123	N9	VCC
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	53	65	F11	92	77	N7	125	P8	I/O
		CS1 (I)			54	66	E11	93	78	P6	126	R8	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	55	67	E10	94	79	M6	131	R7	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	56	70	D10	98	83	M5	137	R5	I/O
		RDY/BUSY	RCLK	RCLK	57	71	C11	99	84	N4	138	P5	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	58	72	B11	100	85	N2	143	R3	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	59	73	C10	1	86	M3	144	N4	I/O
CCLK (I)	CCLK	CCLK	CCLK	CCLK	60	74	A11	2	87	P1	145	R2	CCLK (I)
		WS (I)	A0	A0	61	75	B10	5	90	M2	148	P2	I/O
		CS2 (I)	A1	A1	62	76	B9	6	91	N1	149	M3	I/O
			A2	A2	63	77	A10	8	93	L2	152	P1	I/O
			A3	A3	64	78	A9	9	94	L1	153	N1	I/O
			A15	A15	65	81	B6	12	97	K1	156	M1	I/O
			A4	A4	66	82	B7	13	98	J2	157	L2	I/O
			A14	A14	67	83	A7	14	99	H1	160	K2	I/O
			A5	A5	68	84	C7	15	100	H2	161	K1	I/O
GND	GND	GND	GND	GND	1	1	C6	16	1	H3	164	J3	GND
			A13	A13	2	2	A6	17	2	G2	2	H2	I/O
			A6	A6	3	3	A5	18	3	G1	3	H1	I/O
			A12	A12	4	4	B5	19	4	F2	8	F2	I/O
			A7	A7	5	5	C5	20	5	E1	9	E1	I/O
			A11	A11	6	8	A3	23	8	D1	12	D1	I/O
			A8	A8	7	9	A2	24	9	D2	13	C1	I/O
			A10	A10	8	10	B3	25	10	B1	16	E3	I/O
			A9	A9	9	11	A1	26	11	C2	17	C2	I/O
					X	X	X	X	X				XC3020
					X	X	X	X	X				XC3030
						X	X	X	X	X			XC3042
										X			XC3064
											X	X	XC3090

AVAILABLE PACKAGES

REPRESENTS A 50KΩ TO 100KΩ PULL-UP

* INIT IS AN OPEN DRAIN OUTPUT DURING CONFIGURATION

(I) REPRESENTS AN INPUT

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Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electrically identical. Generic I/O pins are not shown.

XC3000 Family 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

68 PLCC	XC-3020* XC-3030, XC-3042	84 PLCC	84 PGA
10	PWRDN	12	B2
11	TCLKIN-I/O	13	C2
n.c.	I/O*	14	B1
12	I/O	15	C1
13	I/O	16	D2
—	I/O	17	D1
14	I/O	18	E3
15	I/O	19	E2
16	I/O	20	E1
17	I/O	21	F2
18	Vcc	22	F3
19	I/O	23	G3
—	I/O	24	G1
20	I/O	25	G2
21	I/O	26	F1
22	I/O	27	H1
—	I/O	28	H2
23	I/O	29	J1
24	I/O	30	K1
25	M1-RDATA	31	J2
26	M0-RTRIG	32	L1
27	M2-I/O	33	K2
28	HDC-I/O	34	K3
29	I/O	35	L2
30	LDC-I/O	36	L3
31	I/O	37	K4
n.c.	I/O*	38	L4
32	I/O	39	J5
33	I/O	40	K5
n.c.	I/O*	41	L5
34	INIT-I/O	42	K6
35	GND	43	J6
36	I/O	44	J7
37	I/O	45	L7
38	I/O	46	K7
39	I/O	47	L6
40	I/O	48	L8
41	I/O	49	K8
n.c.	I/O*	50	L9
n.c.	I/O*	51	L10
42	I/O	52	K9
43	XTL2(IN)-I/O	53	L11

68 PLCC	XC-3020* XC-3030, XC-3042	84 PLCC	84 PGA
44	RESET	54	K10
45	DONE-PG	55	J10
46	D7-I/O	56	K11
47	XTL1(OUT)-BCLKIN-I/O	57	J11
48	D6-I/O	58	H10
—	I/O	59	H11
49	D5-I/O	60	F10
50	CS0-I/O	61	G10
51	D4-I/O	62	G11
—	I/O	63	G9
52	Vcc	64	F9
53	D3-I/O	65	F11
54	CS1-I/O	66	E11
55	D2-I/O	67	E10
—	I/O	68	E9
n.c.	I/O*	69	D11
56	D1-I/O	70	D10
57	RDY/BUSY-RCLK-I/O	71	C11
58	D0-DIN-I/O	72	B11
59	DOUT-I/O	73	C10
60	CCLK	74	A11
61	A0-WS-I/O	75	B10
62	A1-CS2-I/O	76	B9
63	A2-I/O	77	A10
64	A3-I/O	78	A9
n.c.	I/O*	79	B8
n.c.	I/O*	80	A8
65	A15-I/O	81	B6
66	A4-I/O	82	B7
67	A14-I/O	83	A7
68	A5-I/O	84	C7
1	GND	1	C6
2	A13-I/O	2	A6
3	A6-I/O	3	A5
4	A12-I/O	4	B5
5	A7-I/O	5	C5
n.c.	I/O*	6	A4
n.c.	I/O*	7	B4
6	A11-I/O	8	A3
7	A8-I/O	9	A2
8	A10-I/O	10	B3
9	A9-I/O	11	A1

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

* Indicates unconnected package pins for the XC3020.

XC3000 Family 100-Pin QFP Pinouts

PIN No.		XC3020 XC3030 XC3042
CQFP	PQFP	
1	16	GND
2	17	A13-I/O
3	18	A6-I/O
4	19	A12-I/O
5	20	A7-I/O
6	21	I/O*
7	22	I/O*
8	23	A11-I/O
9	24	A8-I/O
10	25	A10-I/O
11	26	A9-I/O
12	27	Vcc*
13	28	GND*
14	29	$\overline{\text{PWRDN}}$
15	30	I/O
16	31	I/O**
17	32	I/O*
18	33	I/O*
19	34	I/O
20	35	I/O
21	36	I/O
22	37	I/O
23	38	I/O
24	39	I/O
25	40	I/O
26	41	Vcc
27	42	I/O
28	43	I/O
29	44	I/O
30	45	I/O
31	46	I/O
32	47	I/O
33	48	I/O
34	49	I/O

PIN No.		XC3020 XC3030 XC3042
CQFP	PQFP	
35	50	I/O*
36	51	I/O*
37	52	M1-RD
38	53	GND*
39	54	MO-RT
40	55	Vcc*
41	56	M2-I/O
42	57	HDC-I/O
43	58	I/O
44	59	LDC-I/O
45	60	I/O*
46	61	I/O
47	62	I/O
48	63	I/O
49	64	I/O
50	65	$\overline{\text{INIT}}$-I/O
51	66	GND
52	67	I/O
53	68	I/O
54	69	I/O
55	70	I/O
56	71	I/O
57	72	I/O
58	73	I/O
59	74	I/O*
60	75	I/O*
61	76	XTAL2-I/O
62	77	GND*
63	78	$\overline{\text{RESET}}$
64	79	Vcc*
65	80	DONE-$\overline{\text{PG}}$
66	81	D7-I/O
67	82	XTAL1-I/O
68	83	D6-I/O

PIN No.		XC3020 XC3030 XC3042
CQFP	PQFP	
69	84	I/O*
70	85	I/O*
71	86	I/O
72	87	D5-I/O
73	88	$\overline{\text{CS0}}$-I/O
74	89	D4-I/O
75	90	I/O
76	91	Vcc
77	92	D3-I/O
78	93	$\overline{\text{CS1}}$-I/O
79	94	D2-I/O
80	95	I/O
81	96	I/O*
82	97	I/O*
83	98	D1-I/O
84	99	RCLK-$\overline{\text{BUSY}}$/RDY-I/O
85	100	DO-DIN-I/O
86	1	DOUT-I/O
87	2	CCLK
88	3	Vcc*
89	4	GND*
90	5	AO-$\overline{\text{WS}}$-I/O
91	6	A1-CS2-I/O
92	7	I/O*
93	8	A2-I/O
94	9	A3-I/O
95	10	I/O*
96	11	I/O*
97	12	A15-I/O
98	13	A4-I/O
99	14	A14-I/O
100	15	A5-I/O

Unprogrammed IOBs have a default pull-up.
This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew limited.
* Indicates unconnected package pins for the XC3020.
** Indicates unconnected package pins for the XC3020 and the XC3030.

Table 2d. XC3000 Family 132 Pin PGA Pinouts

PGA Pin Number	XC-3042 XC-3064	PGA Pin Number	XC-3042 XC-3064	PGA Pin Number	XC-3042 XC-3064	PGA Pin Number	XC-3042 XC-3064
C4	GND	B13	M1-$\overline{RD}$	P14	$\overline{RESET}$	M3	DOUT-I/O
A1	$\overline{PWRDN}$	C11	GND	M11	VCC	P1	CCLK
C3	I/O	A14	M0-RT	N13	DONE-$\overline{PG}$	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O.	C13	M2-I/O	P13	XTAL1-I/O	M2	A0-$\overline{WS}$-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	$\overline{LDC}$-I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	$\overline{CS0}$-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	$\overline{INIT}$-I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	$\overline{CS1}$-I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RCLK-$\overline{BUSY}$/RDY-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTAL2-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

* Indicates unconnected package pins for the XC3042.

XC3000 Family 164-Pin CQFP Pinouts

CQFP Pin Number	XC-3064 XC-3090
20	PWRDN
21	TCLKIN-I/O
22	I/O*
23	I/O*
24	I/O
25	I/O*
26	I/O
27	I/O*
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	GND
42	Vcc
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O*
58	I/O
59	I/O*
60	I/O

CQFP Pin Number	XC-3064 XC-3090
61	I/O*
62	M1-RDATA
63	GND
64	M0-RTRIG
65	Vcc
66	M2-I/O
67	HDC-I/O
68	I/O
69	I/O
70	I/O
71	LDC-I/O
72	I/O*
73	I/O
74	I/O*
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	INIT-I/O
82	Vcc
83	GND
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O*
97	I/O
98	I/O*
99	XTAL2(IN)-I/O
100	GND
101	RESET
102	Vcc

CQFP Pin Number	XC-3064 XC-3090
103	DONE-PG
104	D7-I/O
105	XTAL1(OUT)-BCLKIN-I/O
106	I/O*
107	I/O
108	I/O
109	D6-I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D5-I/O
116	CS0-I/O
117	I/O*
118	I/O
119	I/O*
120	I/O
121	D4-I/O
122	I/O
123	Vcc
124	GND
125	D3-I/O
126	CS1-I/O
127	I/O
128	I/O*
129	I/O
130	I/O*
131	D2-I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	D1-I/O
138	RDY/BUSY-RCLK-I/O
139	I/O
140	I/O*
141	I/O
142	I/O*

CQFP Pin Number	XC-3064 XC-3090
143	D0-DIN-I/O
144	DOUT-I/O
145	CCLK
146	Vcc
147	GND
148	A0-WS-I/O
149	A1-CS2-I/O
150	I/O
151	I/O
152	A2-I/O
153	A3-I/O
154	I/O
155	I/O
156	A15-I/O
157	A4-I/O
158	I/O
159	I/O
160	A14-I/O
161	A5-I/O
162	I/O*
163	I/O*
164	GND
1	Vcc
2	A13-I/O
3	A6-I/O
4	I/O
5	I/O*
6	I/O
7	I/O*
8	A12-I/O
9	A7-I/O
10	I/O
11	I/O
12	A11-I/O
13	A8-I/O
14	I/O
15	I/O
16	A10-I/O
17	A9-I/O
18	Vcc
19	GND

Unprogrammed IOBs have a default pull-up.
This Prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-limited.
* Indicates unconnected package pins for the XC-3064.

XC3000 Family 175-Pin PGA Pinouts

PGA Pin Number	XC-3090
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	**GND**
D9	**VCC**
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC-3090
D13	I/O
B14	M1-RDATA
C14	**GND**
B15	M0-RTRIG
D14	**VCC**
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	LDC-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	INIT-I/O
H14	**VCC**
J14	**GND**
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTAL2(IN)-I/O
N14	**GND**
R15	RESET
P14	**VCC**

PGA Pin Number	XC-3090
R14	DONE-PG
N13	D7-I/O
T14	XTAL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	CS0-I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	**VCC**
N8	**GND**
P8	D3-I/O
R8	CS1-I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/BUSY-RCLK-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O

PGA Pin Number	XC-3090
R3	D0-DIN-I/O
N4	DOUT-I/O
R2	CCLK
P3	**VCC**
N3	**GND**
P2	A0-WS-I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	**GND**
H3	**VCC**
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	**VCC**
C3	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected.
Pin A1 does not exist.

PARAMETRICS

Absolute Maximum Ratings			Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to Vcc + 0.5	V
V_{TS}	Voltage applied to three-state output	–0.5 to Vcc + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 sec @ 1/16 in.)	+ 260	°C
T_J	Junction temperature plastic	+ 125	°C
	Junction temperature ceramic	+ 150	°C

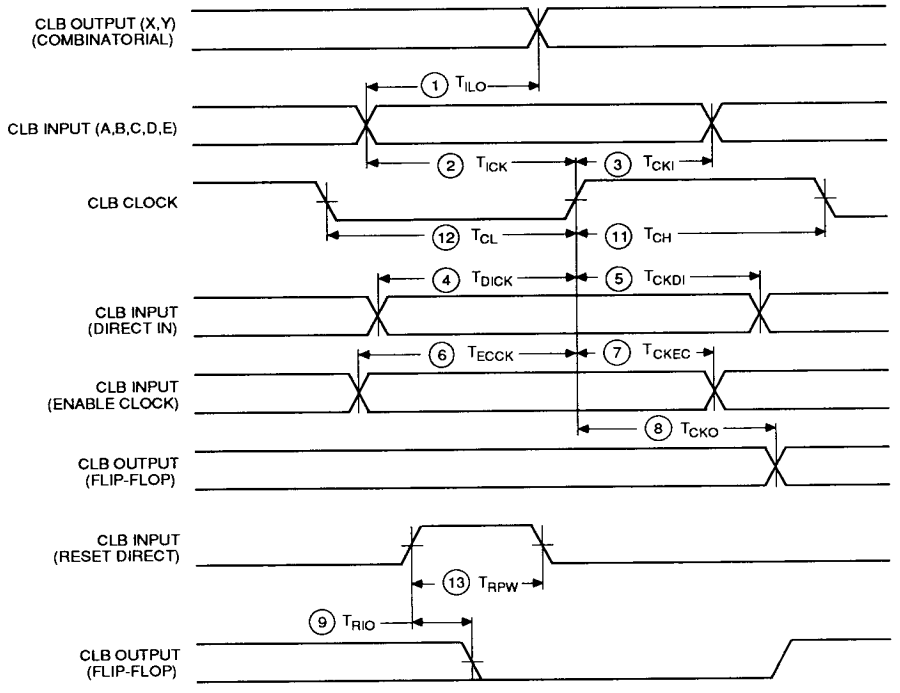
*Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions				Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	–40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	–55°C to 125°C	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration			2.0	Vcc	V
V_{ILT}	Low-level input voltage — TTL configuration			0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration			70%	100%	Vcc
V_{ILC}	Low-level input voltage — CMOS configuration			0	20%	Vcc
T_{IN}	Input signal transition time				250	ns

Electrical Characteristics Over Operating Conditions			Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, Vcc min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, Vcc min)			0.32	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, Vcc min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, Vcc min)			0.37	V
V_{OH}	High-level output voltage (@I_{OH} = –4.0 mA, Vcc min)	Military	3.7		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, Vcc min)			0.4	V
I_{CCPD}	Power-down supply current (Vcc = 5.0 V @ 70°C)	XC3020		500	µA
		XC3030		800	µA
		XC3042		1150	µA
		XC3064		1650	µA
		XC3090		2500	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1]				
	Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	mA
I_{IL}	Leakage Current Commercial/Industrial Temperature		–10	+10	µA
	Leakage Current Military –55°C to 125°C		–20	+20	µA
C_{IN}	Input capacitance, all packages except PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic LOW		0.4	3.4	mA

Note: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at Vcc or GND, and the LCA configured with a MAKEBITS "tie" option. See LCA power chart for additional activity dependent operating component.

CLB SWITCHING CHARACTERISTIC GUIDELINES



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BUFFER (Internal) SWITCHING CHARACTERISTIC GUIDELINES

Description	Symbol	-50 Min	-50 Max	-70 Min	-70 Max	-100 Min	-100 Max	Units
Global and Alternate Clock Distribution**								
Either: **Normal** IOB input pad to clock buffer input	T_{PID}		9		6		4	ns
Or: **Fast** (CMOS only) input pad to clock buffer input	T_{PIDC}		5		3		2	ns
Plus: Clock buffer input to any clock k			9		6		5	ns
TBUF driving a Horizontal Longline (L.L.)**								
I to L.L. while T is Low (buffer active)	T_{ID}		8		5		4	ns
T↓ to L.L. active and valid	T_{ON}		15		9		7	ns
T↑ to L.L. (inactive) with single pull-up resistor	T_{PUS}		34		22		14	ns
with pair of pull-up resistors	T_{PUF}		17		11		7	ns
BIDI								
Bi-directional buffer delay			6		4		3	ns

** Timing is based on the XC3020, for other devices see XACT timing calculator.

CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

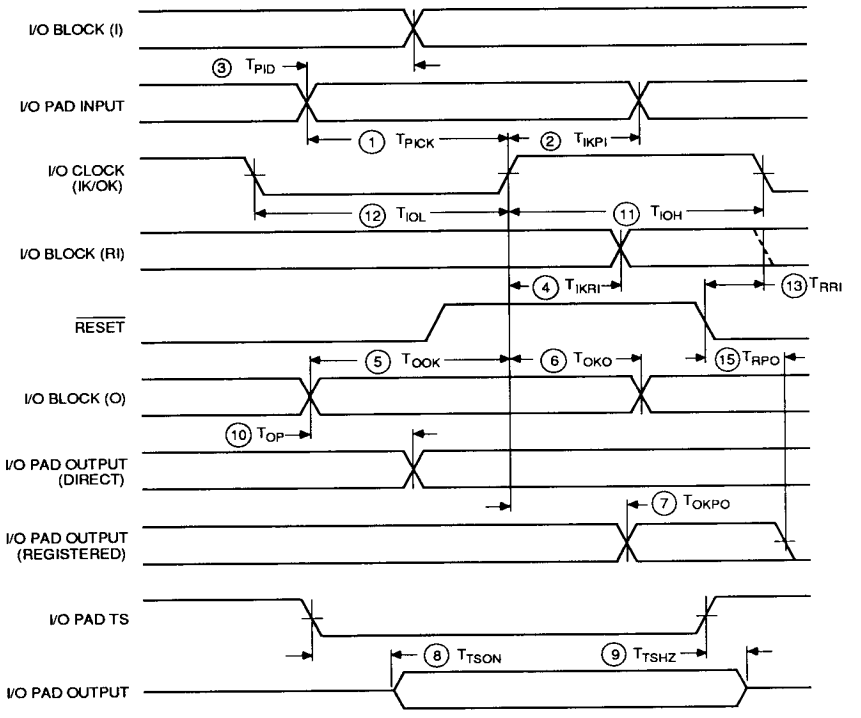
Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching characteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

	Speed Grade		-50		-70		-100		Units
Description	Symbol		Min	Max	Min	Max	Min	Max	
Combinatorial Delay Logic Variables a, b, c, d, e, to outputs x, y	1	TILO		14		9		7	ns
Sequential delay Clock k to outputs x, y Clock k to outputs x,y when Q is returned through function generators F or G to drive x, y	8	TCKO		12 23		8 15		7 12	ns ns
Set-up time before clock K Logic Variables a, b, c, d, e Data In di Enable Clock ec Reset Direct inactive rd	2 4 6	TICK TDICK TECCK	12 8 10 2		8 5 7 1		7 4 5 1		ns ns ns ns
Hold Time after clock k Logic Variables a, b, c, d, e Data In di Enable Clock ec	3 5 7	TCKI TCKDI TCKEC	0 6 0		0 4 0		0 2 0		ns ns ns
Clock Clock High time* Clock Low time* Max. flip-flop toggle rate*	11 12	TCH TCL FCLK	9 9 50		7 7 70		5 5 100		ns ns MHz
Reset Direct (rd) rd width delay from rd to outputs x, y	13 9	TRPW TRIO	12	 12	8	 8	7	 7	ns ns
Master Reset (MR) MR width delay from MR to outputs x, y		TMRW TMRQ	38	 30	25	 20	21	 17	ns ns

* These timing limits are based on calculations.

Note: The CLB K to Q output delay (TCKO, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (TCKDI, #5) of any CLB on the same die.

IOB SWITCHING CHARACTERISTIC GUIDELINES



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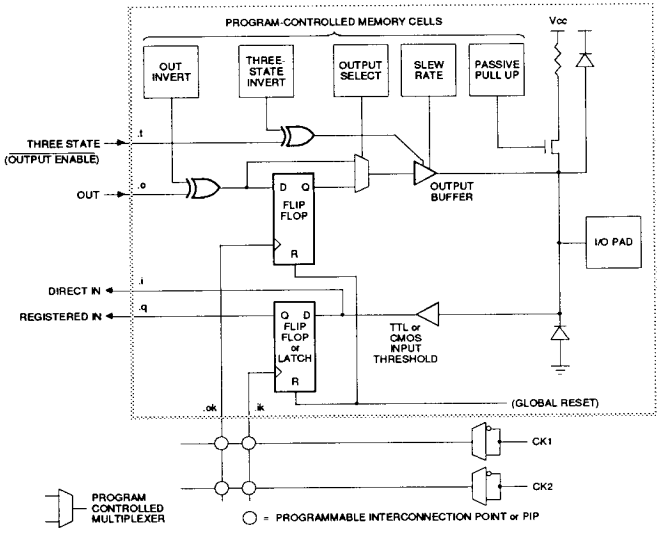


IOB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching charcteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

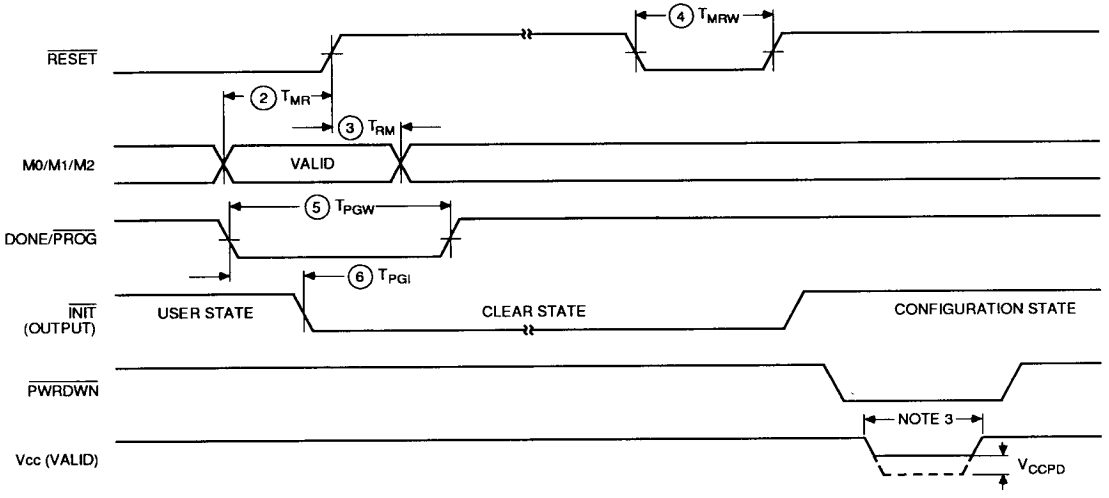
			-50		-70		-100		Units
Description	Symbol		Min	Max	Min	Max	Min	Max	
Propagation Delays (Input)									
Pad to Direct In (i)	3	T_{PID}		9		6		4	ns
Pad to Registered In (q) with latch transparent		T_{PTG}		34		21		17	ns
Clock (ik) to Registered In (q)	4	T_{IKRI}		11		7		6	ns
Set-up Time (Input)									
Pad to Clock (ik) set-up time	1	T_{PICK}	30		20		17		ns
Propagation Delays (Output)									
Clock (ok) to Pad (fast)	7	T_{OKPO}		18		13		10	ns
same (slew rate limited)	7	T_{OKPO}		43		33		27	ns
Output (o) to Pad (fast)	10	T_{OPF}		15		9		6	ns
same (slew-rate limited)	10	T_{OPS}		40		29		23	ns
Three-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		12		8		8	ns
same (slew-rate limited)	9	T_{TSHZ}		37		28		25	ns
Three state to Pad active and valid (fast)	8	T_{TSON}		20		14		12	ns
same (slew -rate limited)	8	T_{TSON}		45		34		29	ns
Set-up and Hold Times (Output)									
Output (o) to clock (ok) set-up time	5	T_{OOK}	15		10		9		ns
Output (o) to clock (ok) hold time	6	T_{OKO}	0		0		0		ns
Clock									
Clock High time	11	T_{CH}	9		7		5		ns
Clock Low time	12	T_{CL}	9		7		5		ns
Max. flip-flop toggle rate		F_{CLK}	50		70		100		MHz
Master Reset Delays									
$\overline{\text{RESET}}$ Pad to Registered In (q)	13	T_{RRI}		35		23		20	ns
$\overline{\text{RESET}}$ Pad to output pad	15	T_{RPO}		50		33		28	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).
Typical fast mode output rise/fall times are 2 ns and will increase approximately 2%/pF of additional load.
Typical slew rate limited output rise/fall times are approximately 4 times longer.
A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is 4 times larger.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (.ik)
In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
For a more detailed description see the discussion on "LCA Performance" in the Applications chapter (6-14 to 18).

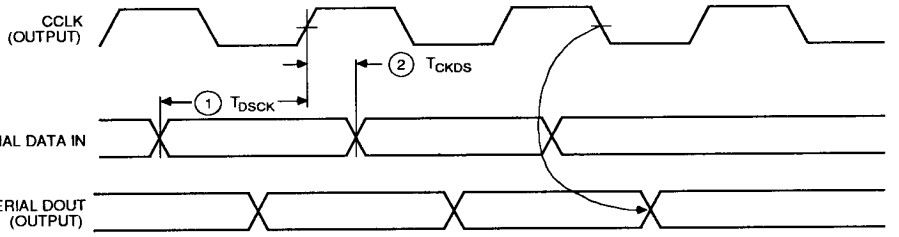
GENERAL LCA SWITCHING CHARACTERISTICS



				-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1	0	1	0	0	0	µs
	M0, M1, M2 hold time required	3	T_{RM}	1		1				µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		6				µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		6		6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7		7		7	µs
PWRDWN (3)	Power Down Vcc		V_{CCPD}	2.0		2.0		2.0		V

Notes: 1. Vcc must rise from 2.0 Volts to Vcc minimum in less than 10 ms for master modes.
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration.
3. PWRDWN transitions must occur during operational Vcc levels.

MASTER SERIAL MODE SWITCHING CHARACTERISTICS GUIDELINES



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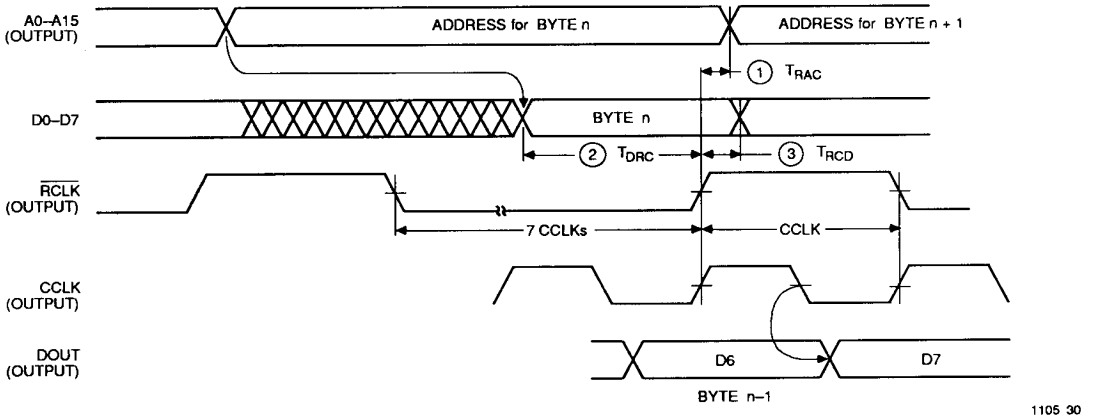
		Speed Grade		-50		-70				Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
CCLK[3]	Data In setup	1	TDSCK	60		60				ns
	Data In hold	2	TCKDS	0		0				ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min. in less than 10 ms, otherwise delay configuration using $\overline{\text{RESET}}$ until Vcc is valid.
2. Configuration can be controlled by holding $\overline{\text{RESET}}$ low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave mode devices is HIGH.
3. Master serial mode timing is based on slave mode testing.

MASTER PARALLEL MODE PROGRAMMING SWITCHING CHARACTERISTIC GUIDELINES

Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching charcteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

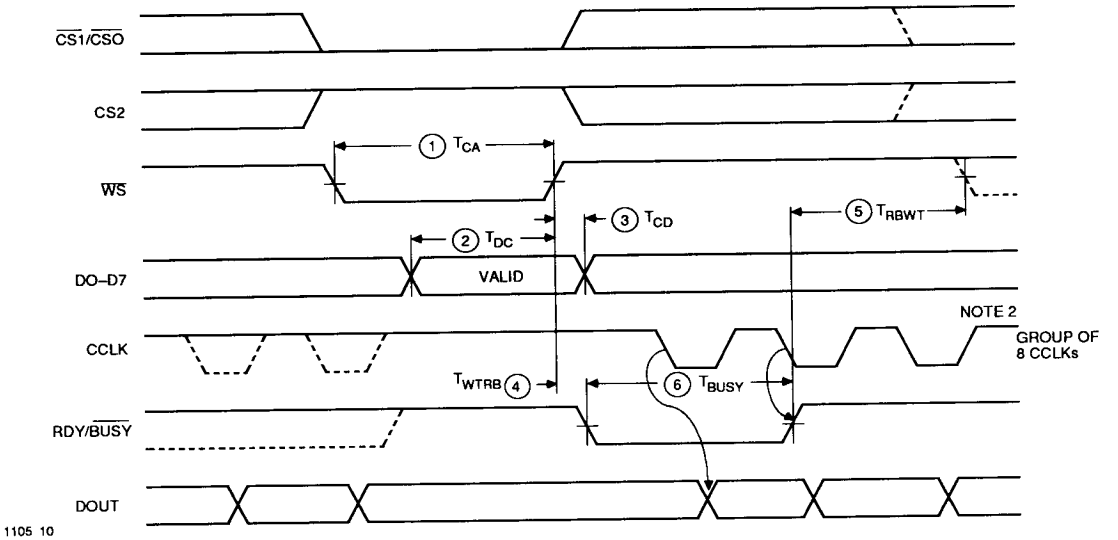


		Symbol		-50		-70				Units
	Description			Min	Max	Min	Max	Min	Max	
RCLK	To address valid	1	TRAC	0	200	0	200			ns
	To data setup	2	TDRC	60		60				ns
	To data hold	3	TRCD	0		0				ns
	RCLK high		TRCH	600		600				ns
	RCLK low		TRCL	4.0		4.0				µs

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min. in less than 10 ms, otherwise delay configuration using $\overline{\text{RESET}}$ until Vcc is valid.
2. Configuration can be contorlled by holding $\overline{\text{RESET}}$ low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave mode devices is HIGH.

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS

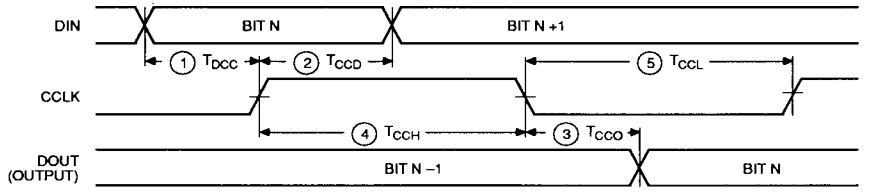


				-50		-70		-100		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
Write	WS Low time reqired	1	TCA	0.5		0.5		0.5		µs
	DIN setup time required	2	TDC	60		60		60		ns
	DIN hold time required	3	TCD	0		0		0		ns
	RDY/BUSY delay after end of WS	4	TWTRB		60		60		60	ns
RDY	Earliest next WS after end of BUSY	5	TRBWT	0		0		0		ns
	BUSY Low time generated	6	TBUSY	4	9	4	9	4	9	CCLK Periods

Notes:
1. Configuration must be delayed until the INIT of all LCAs is HIGH.
2. Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.

This timing diagram shows very relaxed requirements:
Data need not be held beyond the rising edge of WS. BUSY will go active within 60 ns after the end of WS. BUSY will stay active for several microseconds. WS may be asserted immediately after the end of BUSY.

SLAVE MODE PROGRAMMING SWITCHING CHARACTERISTICS



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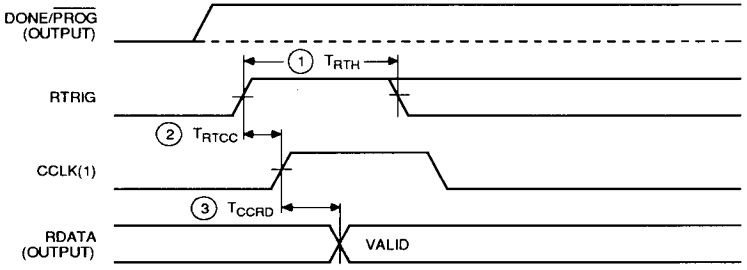
				-50		-70				Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
CCLK	To DOUT	3	TCCO		100		100			ns
	DIN setup	1	TDCC	60		60				ns
	DIN hold	2	TCCD	0		0				ns
	High time	4	TCCH	0.5		0.5				ns
	Low time	5	TCCL	0.5	5.0	0.5	5.0			µs
	Frequency		FCC		1		1			MHz

Note: Configuration must be delayed until the INIT of all LCAs is HIGH.

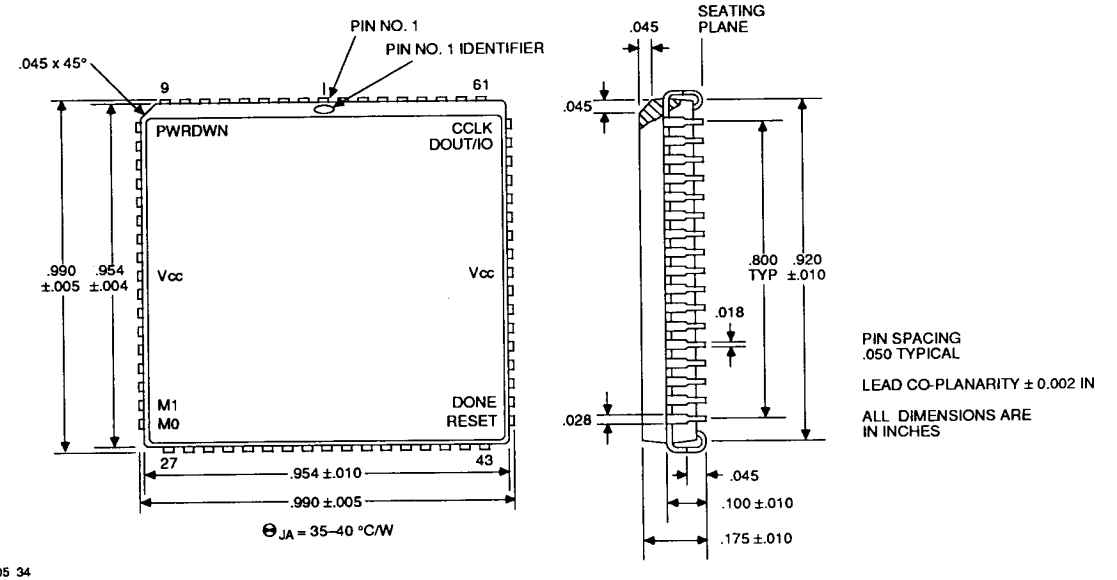
PROGRAM READBACK SWITCHING CHARACTERISTICS



1105 32

				-50		-70				Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RTRIG	RTRIG high	1	TRTH	250		250				ns
CCLK	RTRIG setup	2	TRTCC	10		10				ns
	RDATA delay	3	TCCRD		100		100			ns

Notes: 1. CCLK and DOUT timing are the same as for slave mode.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.



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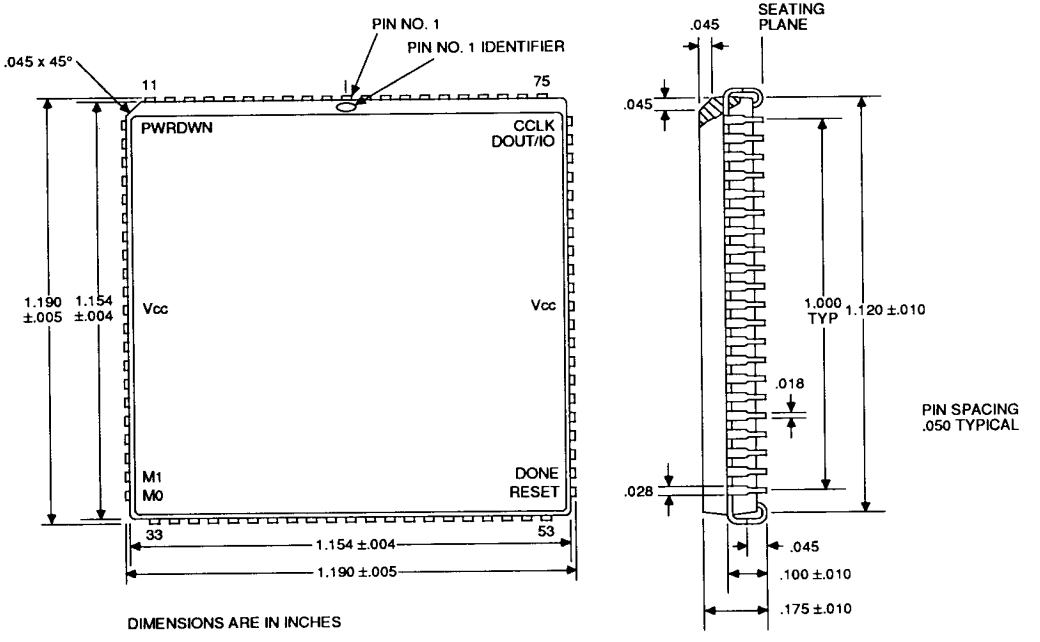
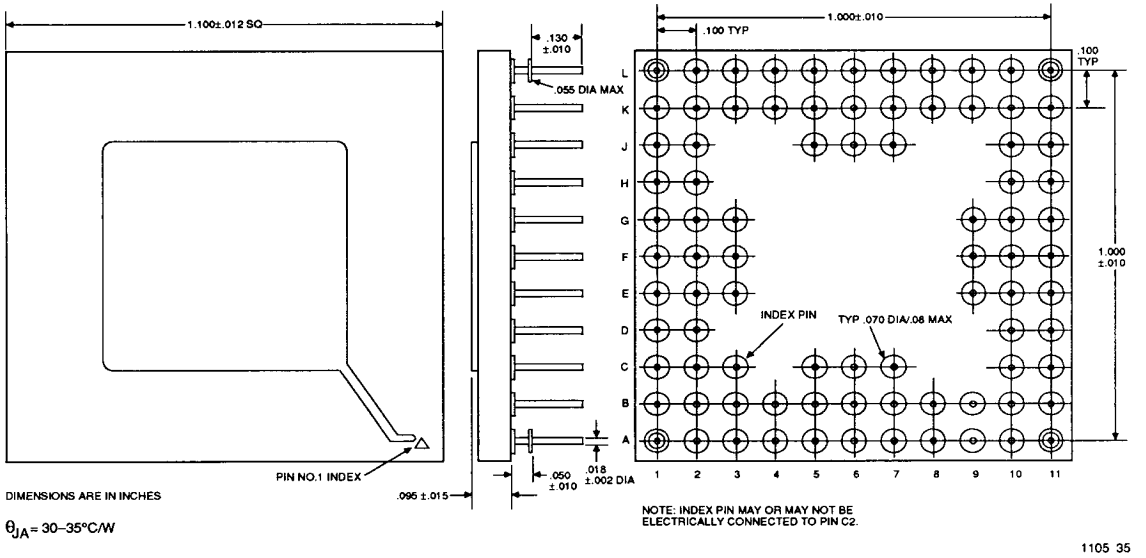
68-Pin PLCC Package



1105 36

84-Pin PLCC Package



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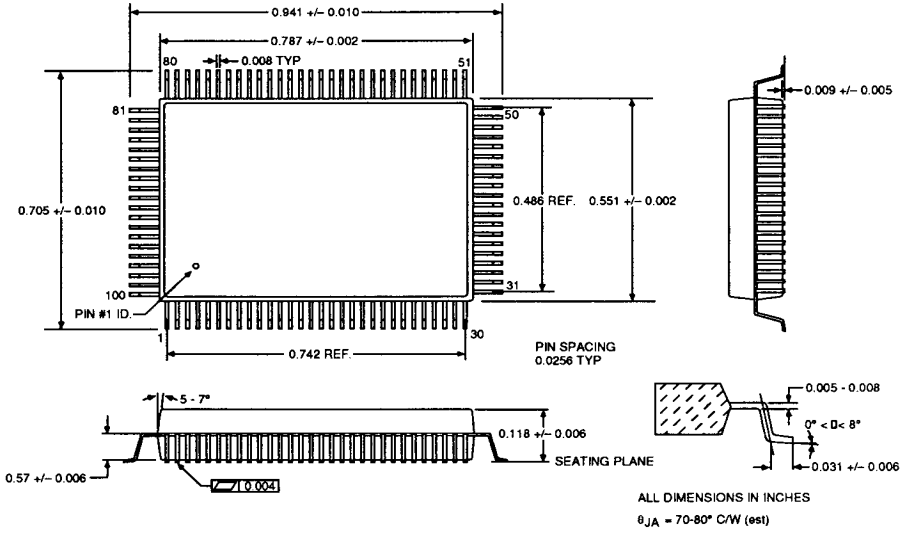
84-Pin PGA Package



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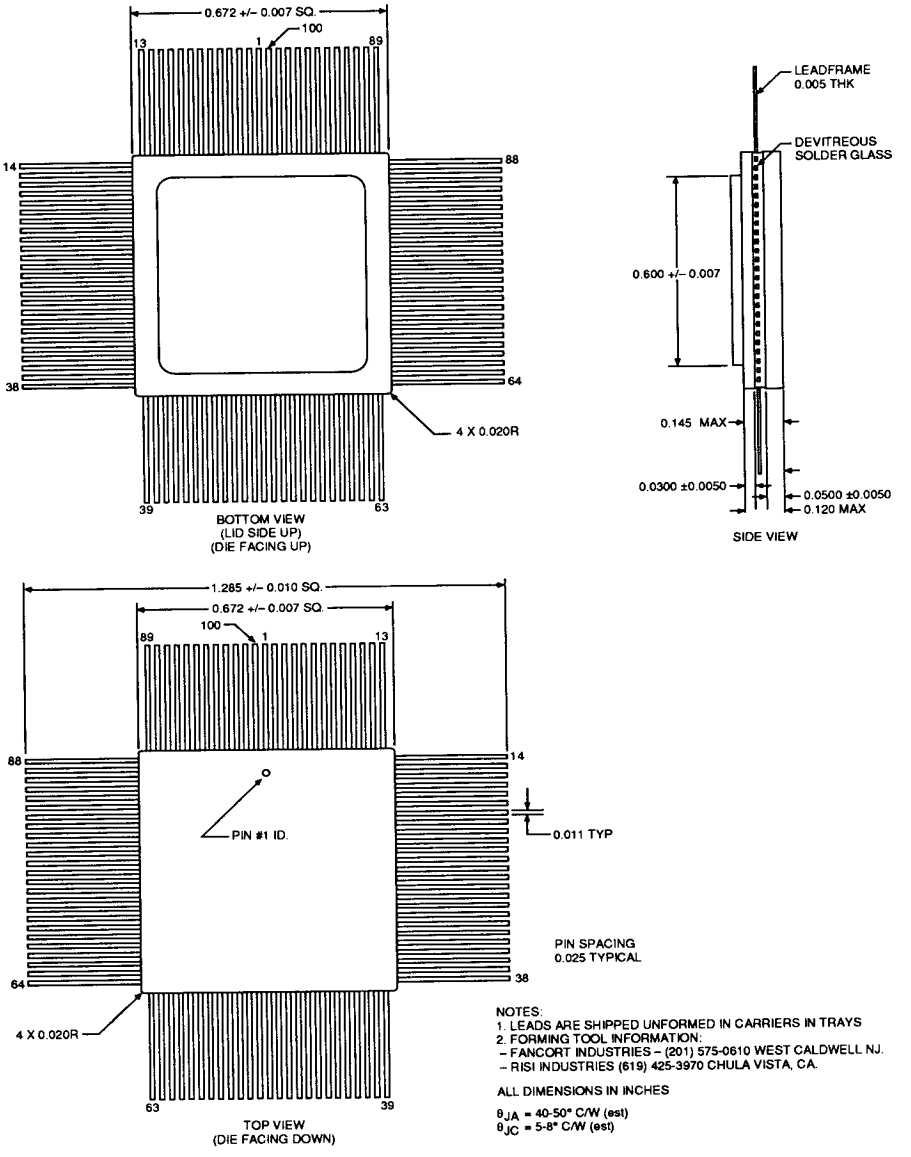
100-Pin PQFP Package



NOTES:
1. LEADS ARE SHIPPED UNFORMED IN CARRIERS IN TRAYS
2. FORMING TOOL INFORMATION:
– FANCORT INDUSTRIES – (201) 575-0610 WEST CALDWELL NJ.
– RISI INDUSTRIES (619) 425-3970 CHULA VISTA, CA.

ALL DIMENSIONS IN INCHES

θ_{JA} = 40-50° C/W (est)
θ_{JC} = 5-8° C/W (est)

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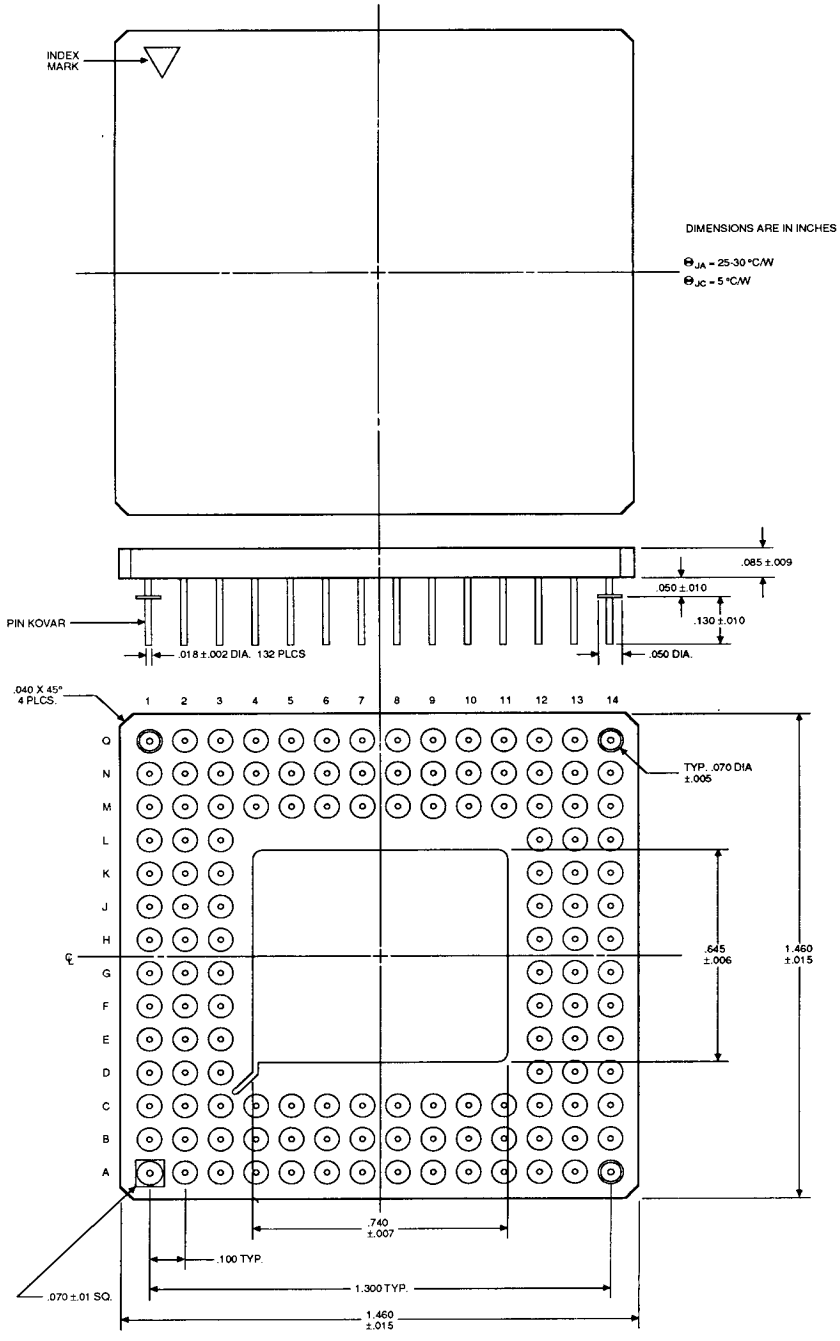
100-Pin CQFP Package



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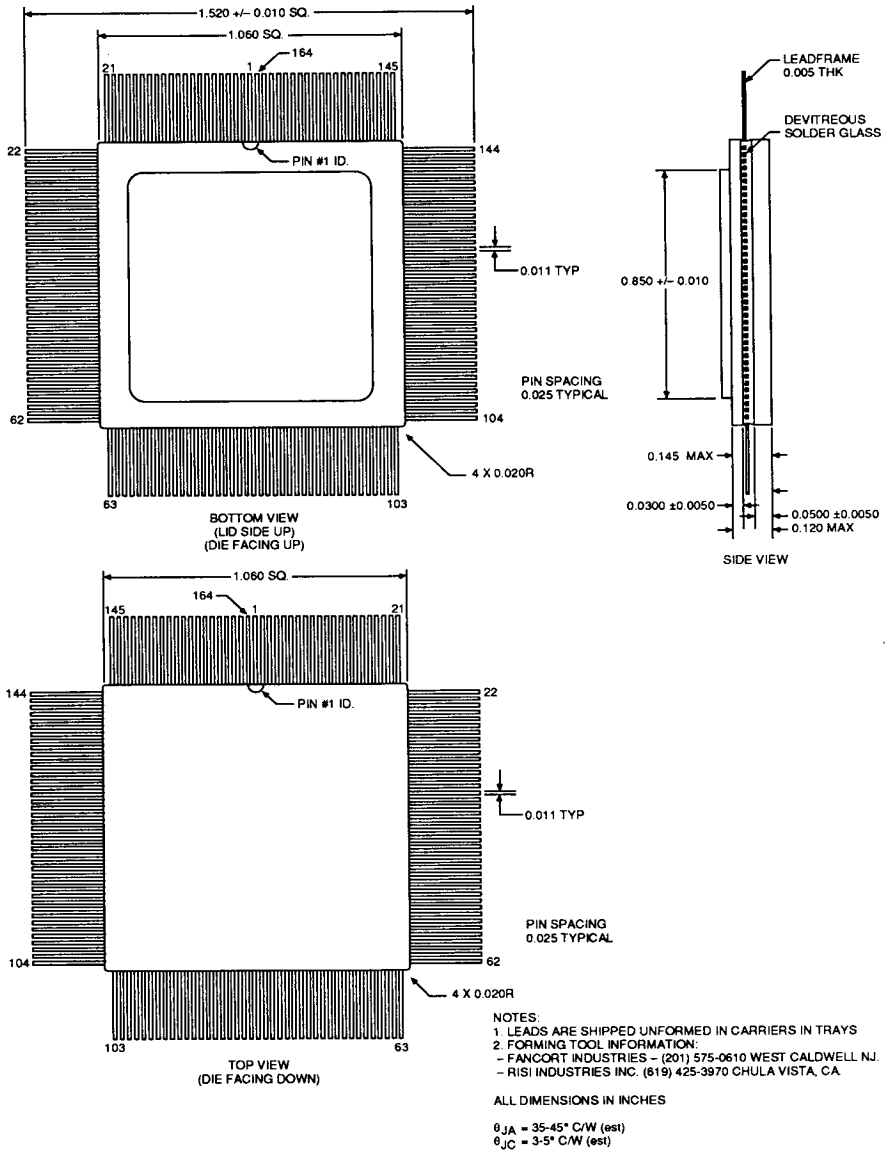
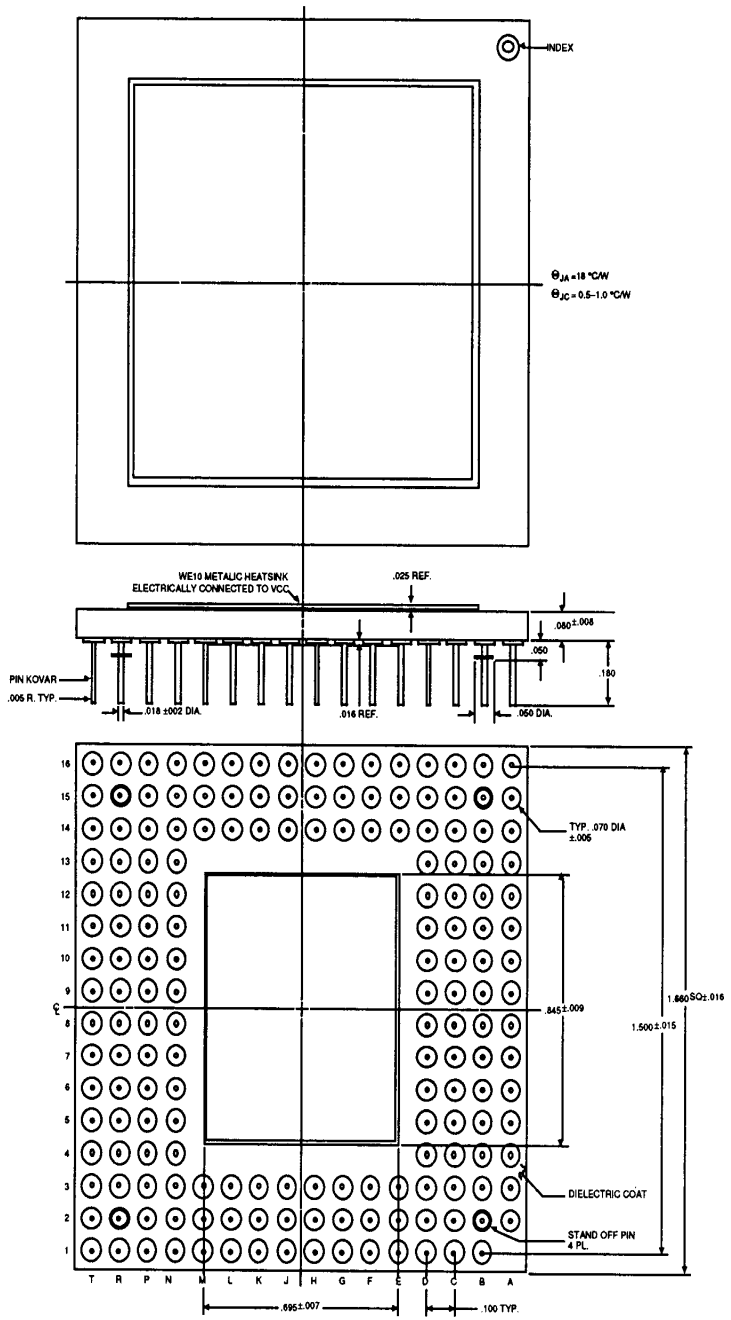
132-Pin PGA Package



164-Pin CQFP Package



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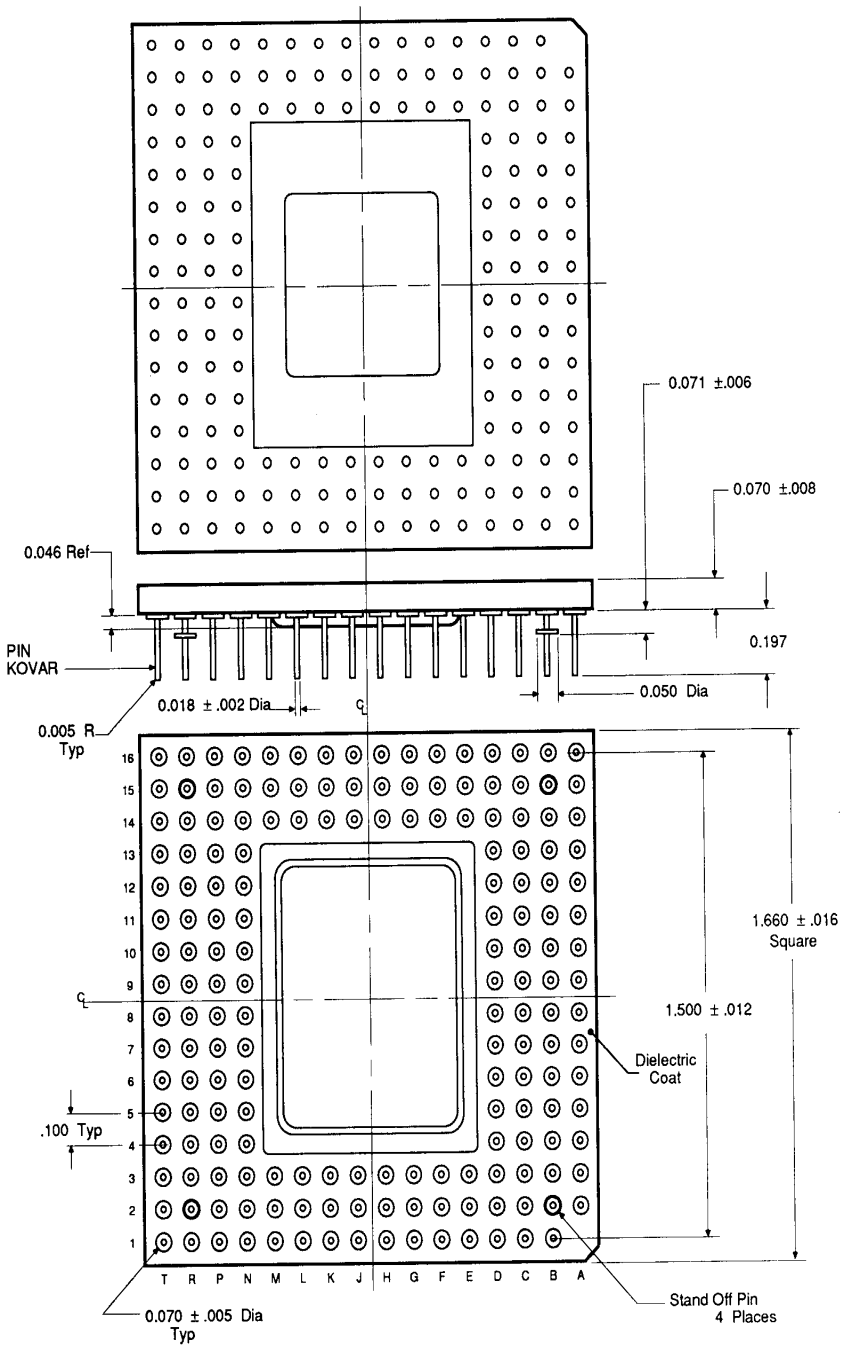
2-54 **175-Pin PGA Package**



1991 01

175-Pin PPGA Package