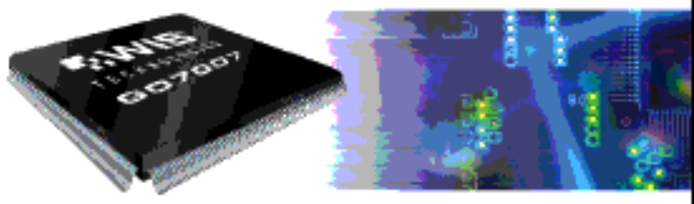
WIS GO7007
Single-Chip Streaming Media Encoder



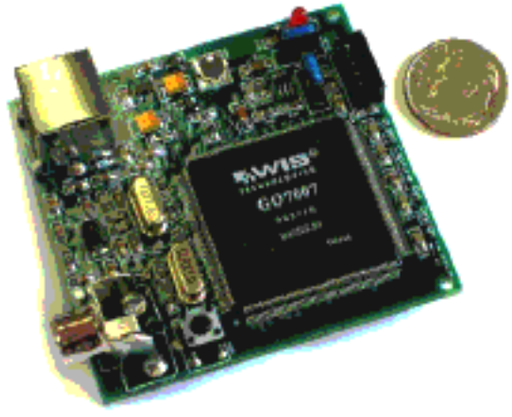
The GO7007 is a monolithic multi-format video compression chip. This high-performance chip uses multiple algorithms to buffer and compress raw video data into video streams. The output video stream is a versatile GoStream™ format that can easily be transcoded by external processors into MPEG-1, MPEG-2, MPEG-4, and H.263 formats. The video streams are output through a Host Parallel Interface (HPI) or a Universal Serial Bus (USB) interface. The GO7007 is capable of delivering streaming video up to full-D1 resolution at a full-motion frame rate, over the Web and emerging broadband networks. It is ideal for a wide range of encoding applications, from DVRs/PVRs to PC/Web cameras.

The WIS GO7007 is a real-time MPEG-4 video compression chip. This high performance encoder enables developers to create and deliver streaming video over the Web, emerging broadband, and mobile networks.

Optimizing Encoding Performance

WIS Technologies' unique encoder architecture provides flexibility to accommodate many different ISO/ITU video standards. The ability to output video streams in almost any standard format greatly benefits upgrade flexibility as standards evolve. Enabling application-level conference bridging and legacy video streaming are additional benefits of the WIS GO7007.

WIS GO chip integration enables a glueless logic interface between the GO7007 and the CMOS image sensors. Included on the chip are SDRAM and USB controllers and I2C and HPI interfaces. Full resolution can be achieved with 4MB PC100 SDRAM to reduce system costs.



Advanced Features:

Output Formats

- MPEG-4 Simple Profile @ L3 plus B-frame support; DivX and WISmp4 compatible
- MPEG-2 MP @ ML
- MPEG-1, H.263, MJPEG
- User-defined formats

Video Input

- CCIR-601 and CCIR-656 YUV (8-bit) 4:2:2 progressive or interlace; all four types of RGB Bayer
- Maximum input size:
  NTSC interlaced: 720 x 480 @ 30fps or 720 x 240 @ 60fps
  PAL: 720 x 576 @ 25fps or 720 x 288 @ 50fps
- Resolution from 64 x 64 to 720 x 576 (16-pixel increments)
- Frame rate up to 30fps (full-D1) or 120fps (CIF)
- WIS-patented RGB Bayer to YUV conversion (high quality)
- WIS-patented de-interlace and 4:2:2 to 4:2:0 conversion
- Optional 1:2 horizontal, vertical, or bi-directional scaling
- Programmable median, low-pass and edge enhancement filtering (up to 10 run-time adjustable parameters)

Video Compression

- WIS-patented Motion Estimation Engine (search range +/-127 horizontal PEL and +/-63 vertical PEL with half-PEL accuracy)
- WIS-patented high precision DCT/IDCT and (de)quantize
- Advanced scene change detection and GOP adjusting
- 48MHz to 96MHz (depending on resolution)
- Programmable GOP structures of I, IP, IBP, IBBP
- WIS-patented advanced MPEG-4 bit-rate control (CBR/VBR) from 1Kbps to 40Mbps

Video Quality and Features

- DVD quality full-D1 video at 2Mbps
- High quality 40Kbps QCIF video for low bandwidth communication
- 2-hour 640 x 352 movie in one 650M CD (average PSNR about 40db)
- Dynamically adjustable bit rate and frame rate to fit variable bandwidths (for Internet communication applications)
- Drivers, SDK, related software (decoding/ transcoding, post-process, Internet-ready software) and sample applications provided
- Most features and parameters are configurable from host (e.g., PC) side
- Internal algorithms of scene change and bit-rate control are upgradeable



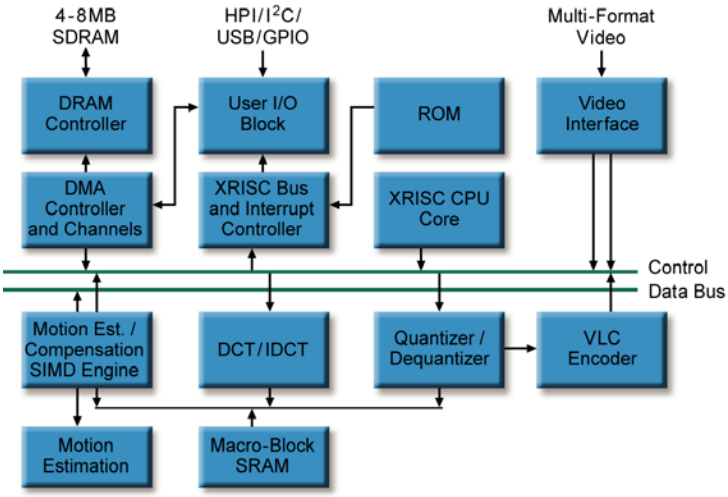
The WIS GO7007 meets the demand for versatility in a broad range of video applications.

Design for Test

- Full scan methodology

Specifications

- 208-pin PQFP (28mm x 28mm)
- 3.3V, 0.18mm, 5-layer metal, single poly
- 4MB or 8MB 32-bit PC100 external SDRAM
- USB1.1 and 16-bit parallel I/F
- Power consumption: 350mW



System-on-Chip Design of the WIS GO7007 Encoder.
Note that most of the blocks are interconnected over a common bus, simplifying the design and encouraging reusability of the intellectual property.

Pin Assignment (top view)

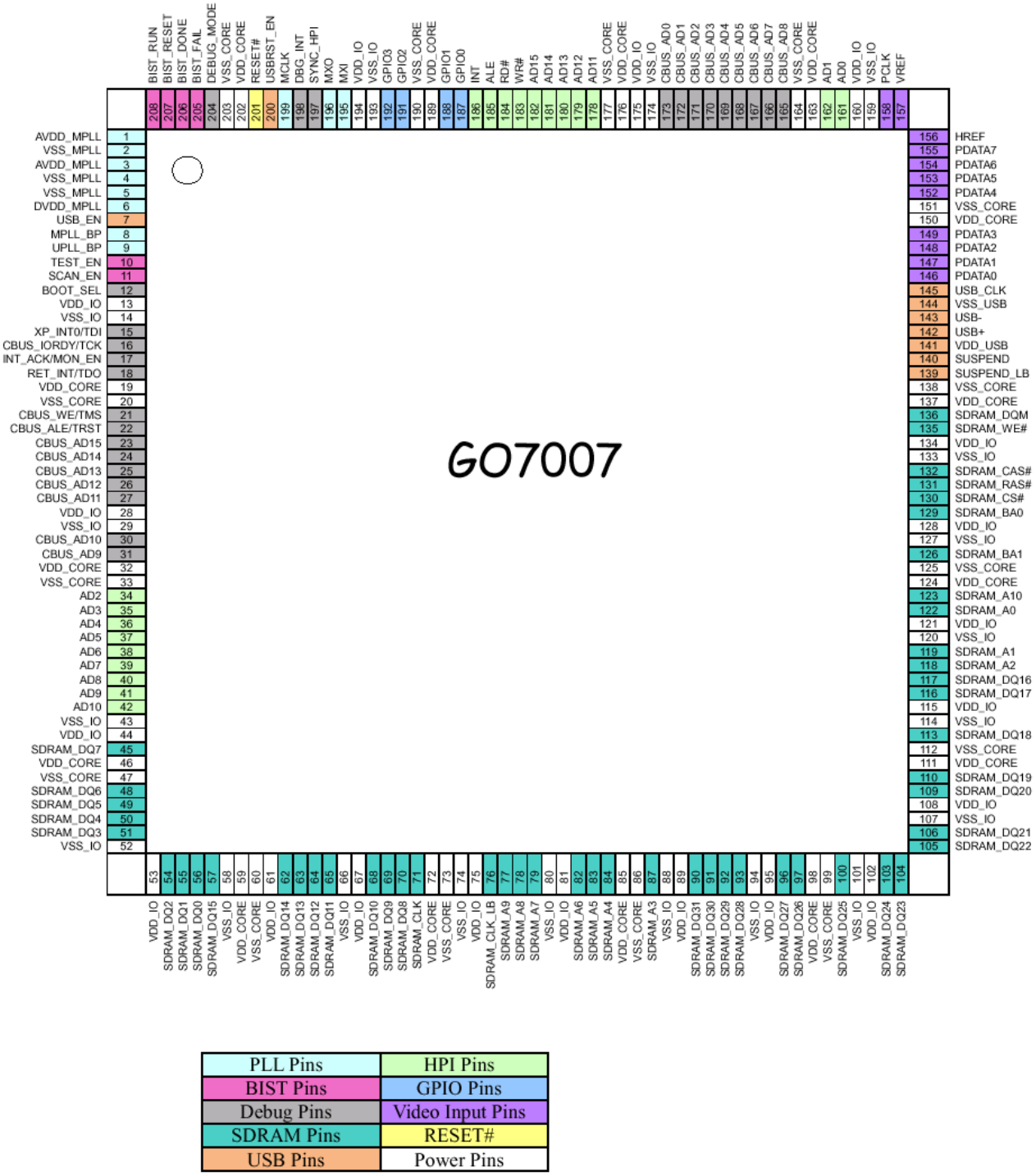


Figure 0-1 GO7007 Pin Diagram

Table 0-1 Pin List

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVDD_MPLL	53	VDD_IO	105	SDRAM_DQ22	157	VREF
2	VSS_MPLL	54	SDRAM_DQ2	106	SDRAM_DQ21	158	PCLK
3	AVDD_MPLL	55	SDRAM_DQ1	107	VSS_IO	159	VSS_IO
4	VSS_MPLL	56	SDRAM_DQ0	108	VDD_IO	160	VDD_IO
5	VSS_MPLL	57	SDRAM_DQ15	109	SDRAM_DQ20	161	AD0
6	DVDD_MPLL	58	VSS_IO	110	SDRAM_DQ19	162	AD1
7	USB_EN	59	VDD_CORE	111	VDD_CORE	163	VDD_CORE
8	MPLL_BP	60	VSS_CORE	112	VSS_CORE	164	VSS_CORE
9	UPLL_BP	61	VDD_IO	113	SDRAM_DQ18	165	CBUS_AD8
10	TEST_EN	62	SDRAM_DQ14	114	VSS_IO	166	CBUS_AD7
11	SCAN_EN	63	SDRAM_DQ13	115	VDD_IO	167	CBUS_AD6
12	BOOT_SEL	64	SDRAM_DQ12	116	SDRAM_DQ17	168	CBUS_AD5
13	VDD_IO	65	SDRAM_DQ11	117	SDRAM_DQ16	169	CBUS_AD4
14	VSS_IO	66	VSS_IO	118	SDRAM_A2	170	CBUS_AD3
15	XP_INT0/TDI	67	VDD_IO	119	SDRAM_A1	171	CBUS_AD2
16	CBUS_IORDY/TCK	68	SDRAM_DQ10	120	VSS_IO	172	CBUS_AD1
17	INT_ACK/MON_EN	69	SDRAM_DQ9	121	VDD_IO	173	CBUS_AD0
18	RET_INT/TDO	70	SDRAM_DQ8	122	SDRAM_A0	174	VSS_IO
19	VDD_CORE	71	SDRAM_CLK	123	SDRAM_A10	175	VDD_IO
20	VSS_CORE	72	VDD_CORE	124	VDD_CORE	176	VDD_CORE
21	CBUS_WE/TMS	73	VSS_CORE	125	VSS_CORE	177	VSS_CORE
22	CBUS_ALE/TRST	74	VSS_IO	126	SDRAM_BA1	178	AD11
23	CBUS_AD15	75	VDD_IO	127	VSS_IO	179	AD12
24	CBUS_AD14	76	SDRAM_CLK_LB	128	VDD_IO	180	AD13
25	CBUS_AD13	77	SDRAM_A9	129	SDRAM_BA0	181	AD14
26	CBUS_AD12	78	SDRAM_A8	130	SDRAM_CS#	182	AD15
27	CBUS_AD11	79	SDRAM_A7	131	SDRAM_RAS#	183	WR#
28	VDD_IO	80	VSS_IO	132	SDRAM_CAS#	184	RD#
29	VSS_IO	81	VDD_IO	133	VSS_IO	185	ALE
30	CBUS_AD10	82	SDRAM_A6	134	VDD_IO	186	INT
31	CBUS_AD9	83	SDRAM_A5	135	SDRAM_WE#	187	GPIO0
32	VDD_CORE	84	SDRAM_A4	136	SDRAM_DQM	188	GPIO1
33	VSS_CORE	85	VDD_CORE	137	VDD_CORE	189	VDD_CORE
34	AD2	86	VSS_CORE	138	VSS_CORE	190	VSS_CORE
35	AD3	87	SDRAM_A3	139	SUSPEND_LB	191	GPIO2
36	AD4	88	VSS_IO	140	SUSPEND	192	GPIO3
37	AD5	89	VDD_IO	141	VDD_USB	193	VSS_IO

38	AD6	90	SDRAM_DQ31	142	USB+	194	VDD_IO
39	AD7	91	SDRAM_DQ30	143	USB-	195	MXI
40	AD8	92	SDRAM_DQ29	144	VSS_USB	196	MXO
41	AD9	93	SDRAM_DQ28	145	USB_CLK	197	SYNC_HPI
42	AD10	94	VSS_IO	146	PDATA0	198	DBG_INT
43	VSS_IO	95	VDD_IO	147	PDATA1	199	MCLK
44	VDD_IO	96	SDRAM_DQ27	148	PDATA2	200	USBRST_EN
45	SDRAM_DQ7	97	SDRAM_DQ26	149	PDATA3	201	RESET#
46	VDD_CORE	98	VDD_CORE	150	VDD_CORE	202	VDD_CORE
47	VSS_CORE	99	VSS_CORE	151	VSS_CORE	203	VSS_CORE
48	SDRAM_DQ6	100	SDRAM_DQ25	152	PDATA4	204	DEBUG_MODE
49	SDRAM_DQ5	101	VSS_IO	153	PDATA5	205	BIST_FAIL
50	SDRAM_DQ4	102	VDD_IO	154	PDATA6	206	BIST_DONE
51	SDRAM_DQ3	103	SDRAM_DQ24	155	PDATA7	207	BIST_RESET
52	VSS_IO	104	SDRAM_DQ23	156	HREF	208	BIST_RUN

Table 0-2 Pin Description

Symbol	Pin #	Pin Type	Description	Note
PLL Pins				
AVDD_MPLL	1, 3	Supply	1.8V Analog power supply for Master clock PLL	
VSS_MPLL	2, 4, 5	Supply	Ground for Master clock PLL	
DVDD_MPLL	6	Supply	1.8V Digital power supply for Master clock PLL	
MPLL_BP	8	Input	Master clock PLL Bypass. When pin is tied to ground, master clock is generated by internal PLL locked to MXI. Otherwise, MCLK is used as master clock input.	
UPLL_BP	9	Input	USB clock PLL Bypass. When pin is tied to ground, USB clock is generated by internal PLL locked to MXI. Otherwise, USB_CLK is used as USB clock input.	1
MXI	195	Input	Oscillator Input	
MXO	196	Output	Usually connected to the crystal	
MCLK	199	Input	Use this Master Clock input pin when Master clock PLL is bypassed.	
Built-In Self Test Pins				
TEST_EN	10	Input	Test Enable. Reserved for manufacturers' use. Connect pin to ground under normal operation.	

SCAN_EN	11	Input	Scan Enable. Reserved for manufacturers' use. Connect pin to ground under normal operation.	
BIST_FAIL	205	Output	Built-In Self Test Fail indicator	
BIST_DONE	206	Output	Built-In Self Test Done indicator	
BIST_RESET	207	Input	Built-In Self Test Reset. Reserved for manufacturers' use. Connect pin to logic 1 under normal operation.	
BIST_RUN	208	Input	Built-In Self Test start. Reserved for manufacturers' use. Connect pin to ground under normal operation.	
Debug Pins			Reserved for manufacturers' use	
XP_INT0/ TDI	15	Output/ Input	When Control Bus monitor is enabled, this pin monitors Internal XRISC Interrupt #0. Otherwise, it is used as Test Data Input for the JTAG interface. If JTAG is not used, a 10kΩ pull-up is required.	
CBUS_IORDY/ TCK	16	Output/ Input	When Control Bus monitor is enabled, this pin monitors the internal Control Bus IO_Ready. Otherwise, it is used as a Test Clock for the JTAG interface. If JTAG is not used, a 10kΩ pull-up is required.	
CBUS_WE/ TMS	21	Output/ Input	When Control Bus monitor is enabled, this pin monitors internal Control Bus Write Enable. Otherwise, it is used as a Test Mode Select for the JTAG interface; a 10kΩ pull-up is required.	
CBUS_ALE/ TRST	22	Output/ Input	When Control Bus monitor is enabled, this pin monitors internal Control Bus Address Latch Enable. Otherwise, it is used as a Test Reset for the JTAG interface; a 10kΩ pull-up is required.	
CBUS_AD15-CBUS_AD0	23-27, 30-31, 165-173	Output	When Control Bus monitor is enabled, these pins are connected to the internal Control Bus Address and Data. When CBUS_ALE is 1, the Address on the Control Bus is output. Otherwise, Data on Control Bus is output.	
DEBUG_MODE	204	Input	10kΩ pull-down is required.	
DBG_INT	198	Input	Reserved; 10kΩ pull-down is required.	
SYNC_HPI	197	Input	Reserved; 10kΩ pull-down is required.	
RET_INT/TDO	18	Output	Reserved in functional mode. In JTAG mode, this pin is the Test Data Output for the JTAG interface.	
INT_ACK/ MON_EN	17	Input	Reserved; 10kΩ pull-down is required.	
BOOT_SEL	12	Input	Reserved; 10kΩ pull-down is required.	

SDRAM Pins				
SDRAM_DQ31-SDRAM_DQ0	90-93, 96, 97, 100, 103-106, 109, 110, 113, 116, 117, 57, 62-65, 68-70, 45, 48-51, 54-56	Input/ Output	SDRAM Data	
SDRAM_A10-SDRAM_A0	123, 77-79, 82-84, 87, 118, 119, 122	Output	SDRAM Address	
SDRAM_BA1-SDRAM_BA0	126, 129	Output	SDRAM Bank Address	
SDRAM_CS#	130	Output	SDRAM Chip Select	
SDRAM_RAS#	131	Output	SDRAM Row Address Select	
SDRAM_CAS#	132	Output	SDRAM Column Address Select	
SDRAM_WE#	135	Output	SDRAM Write Enable	
SDRAM_DQM	136	Output	SDRAM DQ Mask	
SDRAM_CLK	71	Output	SDRAM Clock. Connect this pin to the SDRAM chip clock input pin.	
SDRAM_CLK_LB	76	Input	SDRAM Clock Loop Back. This pin is used to compensate transfer delays on SDRAM signals. Connect this pin to the SDRAM chip clock input pin via a separate route from the SDRAM_CLK connection. See the SDRAM clock scheme in **Error! Reference source not found.**.	
Video Data Input Pins				
PDATA0-PDATA7	146-149, 152-155	Input	Pixel Data Input	
HREF	156	Input	Horizontal Reference. Active edge on this pin indicates beginning of active video data in a horizontal period. The active edge can be configured as a positive or negative edge.	
VREF	157	Input	Vertical Reference. Active edge on this pin indicates beginning of active video data in a vertical period. The active edge can be configured as a positive or negative edge.	
PCLK	158	Input	Pixel Clock	

HPI Pins				
AD0-AD15	161-162, 34-42, 178-182	Input/ Output	HPI Address and Data multiplexed bus.	
INT	186	Output	HPI Interrupt request to external host.	
ALE	185	Input	HPI Address Latch Enable	
RD#	184	Input	HPI Read strobe (active low)	
WR#	183	Input	HPI Write strobe (active low)	
USB Pins				
USB DATA-	143	Input/ Output	USB Data-	
USB DATA+	142	Input/ Output	USB Data+	
USB_CLK	145	Input	48MHz USB Clock input. Use as USB clock input when USB clock PLL is bypassed.	
VDD_USB	144	Supply	VDD for USB; connect to 3.3V power supply.	
VSS_USB	141	Supply	VSS for USB; connect to ground.	
SUSPEND	140	Output	USB Suspend output. This pin is high when GO7007 goes into suspend mode.	
SUSPEND_LB	139	Input	USB Suspend Loop Back. Usually connected to SUSPEND via R-C network for a delayed start of internal clock when GO7007 resumes from suspend state.	
USB_EN	7	Input	USB/HPI Select input. Tying pin to VDD will enable USB functionality and disable HPI interface. To use only HPI interface, tie pin to VSS. Pin status will be sampled only upon power-on reset.	
USBRST_EN	200	Input	USB Reset Enable. Tie pin to logic 1 for USB bus to reset other parts of GO7007. To disable this feature, connect pin to ground. Changing the status of this pin after power-on will have no effect.	
GPIO Pins				
GPIO3-GPIO0	192, 191, 188, 187	Input/ Output	General Purpose I/O pins programmed as input or output on a pin-by-pin basis.	
Reset and Power Supply Pins				
RESET#	201	Input	Global Reset input. Setting pin low (at least 100µs) will reset GO7007 (active low).	

VDD_CORE	202, 189, 176, 163, 150, 137, 124, 111, 98, 85, 72, 59, 46, 32, 19	Supply	1.8V power supply for Core logic.	
VDD_IO	194, 175, 160, 134, 128, 121, 115, 108, 102, 95, 89, 81, 75, 67, 61, 53, 44, 28, 13	Supply	3.3V power supply for IO	
VSS_CORE	203, 190, 177, 164, 151, 138, 125, 112, 99, 86, 73, 60, 47, 33, 20	Supply	Ground for Core logic	
VSS_IO	193, 174, 159, 133, 127, 120, 114, 107, 101, 94, 88, 80, 74, 66, 58, 52, 43, 29, 14	Supply	Ground for IO	

About WIS

WIS Technologies is a privately held, fabless semi-conductor company. At WIS Technologies, an international team of experts in image processing and digital communication create innovative chip technology and software. WIS provides advanced features and unprecedented levels of integration, performance and quality, enabling complete, scalable, and highly configurable multimedia communication systems.

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