

ARCHITECTURE HIGHLIGHTS

Industry Leading GPS Performance

- Builds on high performance SiRFstarI core
- Signal acquisition using 1920 time/frequency search channels
- Wide Area Augmentation System (WAAS) and U.S. Coast Guard Beacon support
- Satellite signal tracking engine to perform GPS acquisition and tracking functions without CPU intervention
- Multipath-mitigation hardware
- Cold Start under 45 seconds

Low Power

- Advanced TricklePower mode for power savings to 98% with no extra parts
- Extreme low power in power down mode, but capable of very fast starts

Maximizes GPS Position Availability

- SingleSat™ updates in reduced visibility
- Superior urban canyon performance
- FoliageLock™ for weak signal tracking

FAMILY HIGHLIGHTS

GSP2e - GPS Digital IC

- Integrated ARM7TDMI up to 50 MHz
- Support 16 and 32 bit data bus operation
- Separate internal and external buses
- On-chip 1Mb EDO DRAM for GPS navigation
- Instruction cache to improve throughput
- Integrated high-precision Real-Time Clock
- Extensive GPS receiver peripherals
- 2 UARTS, high speed serial bus, battery backed SRAM, >40 GPIO

GRF2i - Cost Effective RFIC

- On-chip VCO and reference oscillator
- Single stage L1 to IF down-conversion
- Integrated LNA
- Simplified digital interface

GSW2 Modular Software

- Easily integrated into existing systems
- 90% CPU throughput available for user tasks
- Tunable performance in all applications
- Robust development environment

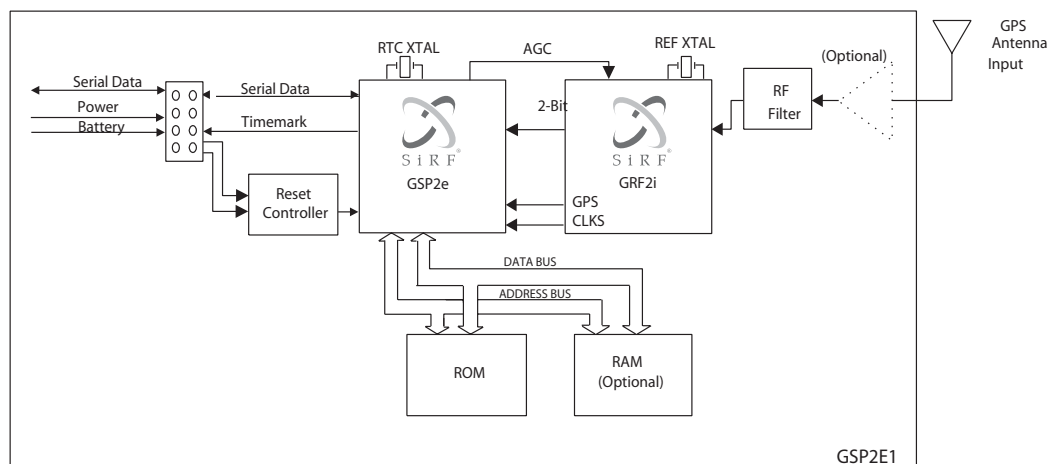
SiRFstarII ARCHITECTURE

SiRFstarII architecture builds on the high-performance SiRFstarI core, adding an acquisition accelerator, differential GPS processor, multipath mitigation hardware and satellite-tracking engine. SiRFstarII delivers major advancements in GPS performance, accuracy, integration, computing power and flexibility. It is the first GPS architecture designed to be available both as a highly integrated chip set configuration and an IP core.

The SiRFstarIIe family consists of the GSP2e highly integrated digital section, GRF2i integrated front end and GSW2e software that provides flexible system architecture for stand-alone GPS based products. A 50MHz ARM7 CPU has sufficient throughput to support extensive user application software and peripherals. The internal satellite signal-tracking engine provides highly accurate GPS measurements and differential corrections and eliminates the need for a high rate GPS interrupt. This makes SiRFstarII architecture the preferred platform for a wide variety of GPS based consumer products.



SiRFstarIIe BLOCK DIAGRAM



GSP2E1

Evaluate

Develop

Build

TECHNICAL SPECIFICATIONS

Position Accuracy (95%)

Autonomous	<10m
WAAS	<5m
Beacon DGPS	<2.5m

Receiver

Tracking	L1, CA code
Channels	12
Max. Update Rate	10Hz
Sensitivity	-172dBW
Max. Altitude	<60,000 ft
Max. Velocity	<1,000 knots
Protocol Support	NMEA, SiRF Binary

Acquisition

Reacquisition Time	100msec
SnapStart	<3sec
Hot Start	<8sec
Warm Start	<38sec
Cold Start	<50sec

Power

Draw - Full Power	<500mW
Draw - TricklePower	<150mW
Voltage	2.7-3.3V (5V I/O capable)

APPLICATIONS

The SiRFstarIIe is a flexible GPS chip set that integrates into a postage-sized receiver. It works well where GPS is the main function, "GPS-centric" or where the design calls for stand-alone GPS functionality. "GPS-centric" applications include handheld GPS, marine GPS, and personal locators. The processing power can be used for such user tasks as running an LCD. The SiRFstarIIe can also be used where a low-cost autonomous GPS is needed such as in vehicle location.

CHIP ORDERING CONFIGURATION

RF CHIP PACKAGES

Chip Name	Chip PN	Package
SiRFstarII GRF2i	1540-0005	LQFP, 48 pin
SiRFstarII GRF2i (QFN)	1540-0204	(LPCC), 32 pin

DIGITAL CHIP PACKAGES

Chip Name	Chip PN	Package
SiRFstarII GSP2e	1540-7400	TQFP, 16-bit, 100 pin
SiRFstarII GSP2e	1540-7401	BGA, 16-bit, 144 pin
SiRFstarII GSP2e	1540-7410	LQFP, 32-bit, 144 pin

For more information, contact your SiRF representative, call our sales force on +1 (408) 467-0410, or visit us at www.sirf.com.

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Mobile Compute



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